

Se pretende controlar la posición vertical de una bola utilizando un sistema de levitación magnético mediante el ajuste de la corriente que circula por la bobina, tal y como se muestra en la figura 1(a).

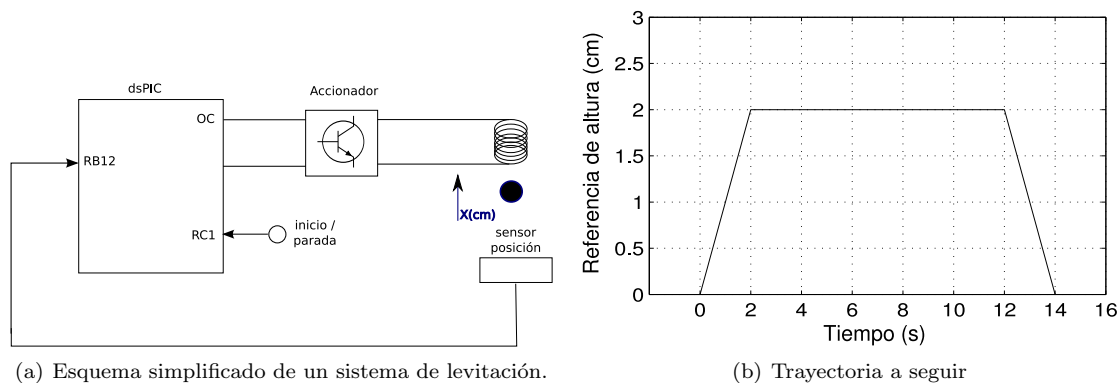


Figura 1: Esquema del sistema de levitación y conexión con el dsPIC.

Para realizar el control se pretende emplear un dsPic 30f6010, con un reloj externo de **20MHz**.

Cada cuestión se debe realizar de forma independiente. Para ello se supondrá en cada una que las variables correspondientes a los apartados anteriores han sido correctamente calculadas. No es necesario repetir en cada cuestión el código desarrollado para las anteriores, sino sólo las modificaciones.

- 2pt.
1. Se desea arrancar el sistema mediante un pulsador conectado a la **línea 1 del puerto C**. Para ello se cambiará el valor de la variable global **activo** cuando dicho pulsador se active durante un tiempo superior a 0,1s. Usar para ello el modo **TGATE** del **Timer2**. Colocar el código en la rutina de interrupción correspondiente. La función **main**, debe realizar la configuración, y posteriormente permanecer en un estado de ahorro de energía.
- 2pt.
2. Programar el conversor AD para tomar datos del sensor de posición mostrado en la figura 1(a) con una frecuencia de muestreo de 750Hz. El sensor tiene una relación $0V \rightarrow 0cm, 5V \rightarrow 3cm$. **Evitar cualquier tipo de espera ocupada**. Suponer el sensor conectado a la **línea 12 del puerto B**. Guardar en un vector llamado **altura** los últimos 16 datos de dicha medida (en cm). Suponer disponibles las funciones:
`void Inicializavector(volatile float vector, int tam)`
`void Desplazavector(volatile float vector, int tam)`
- 1pt.
3. Para eliminar el ruido presente en la medida de la posición de la bola se debe implementar un filtro de media móvil con las últimas 16 datos adquiridos, y guardar los datos en el vector **altura_filtrada**.
- 1pt.
4. Para controlar la posición de la bola, se debe generar una tensión función del error entre la referencia y la medida filtrada. El resultado de la comparación (diferencia) se almacenará en la variable **error**. La señal de error se utilizará para generar la tensión según la ecuación en diferencias dada por la expresión:

$$u_k = K_p \cdot error_k$$
 siendo: $K_p = 2$, y considerando para este apartado una referencia cte de valor $1,5cm$. Guardar el valor de la señal u (tensión) en un vector de tamaño 16 llamado **acc_control**. Programar el código necesario en la rutina de interrupción del conversor A/D.
- 2pt.
5. Para accionar la bobina se debe generar una señal PWM con un duty proporcional al valor de la acción de control (**acc_control**) en el instante actual. Para ello se debe establecer la relación $0V \rightarrow 0\%, 5V \rightarrow 100\%$. Configurar una salida del módulo OC para generar dicha señal, con una frecuencia de modulación de 750Hz.
- 1pt.
6. Como demostración del sistema se pretende realizar un movimiento de despegue suave, levitación sostenida y aterrizaje controlado de la bola, según la figura 1(b). Generar en **tiempo real**, la señal de referencia mostrada en la figura 1(b). Indicar para ello el código que sería necesario añadir a la rutina de interrupción del AD.
- 1pt.
7. ¿Qué hardware sería necesario para controlar la posición de la bola en ambos sentidos?

12.3 Control Registers

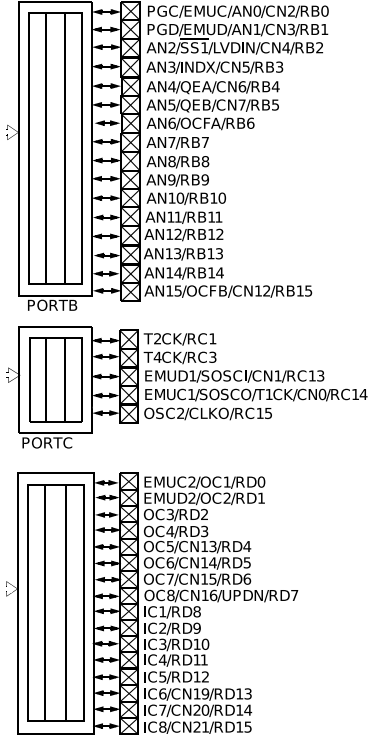
Register 12-1: TxCON: Type A Time Base Register

| | | | | | | | | |
|-------------|-----|-------|-----|-----|-----|-----|-----|-------|
| Upper Byte: | | | | | | | | |
| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | |
| TON | — | TSIDL | — | — | — | — | — | |
| bit 15 | | | | | | | | bit 8 |

| | | | | | | | | |
|-------------|-------|------------|-------|-----|-------|-------|-----|-------|
| Lower Byte: | | | | | | | | |
| U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 | |
| — | TGATE | TCKPS<1:0> | | — | TSYNC | TCS | — | |
| bit 7 | | | | | | | | bit 0 |

- bit 15 **TON:** Timer On Control bit
1 = Starts the timer
0 = Stops the timer
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **TSIDL:** Stop in Idle Mode bit
1 = Discontinue timer operation when device enters Idle mode
0 = Continue timer operation in Idle mode
- bit 12-7 **Unimplemented:** Read as '0'
- bit 6 **TGATE:** Timer Gated Time Accumulation Enable bit
1 = Gated time accumulation enabled
0 = Gated time accumulation disabled
(TCS must be set to '0' when TGATE = 1. Reads as '0' if TCS = 1)
- bit 5-4 **TCKPS<1:0>:** Timer Input Clock Prescale Select bits
11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value
- bit 3 **Unimplemented:** Read as '0'
- bit 2 **TSYNC:** Timer External Clock Input Synchronization Select bit
When TCS = 1:
1 = Synchronize external clock input
0 = Do not synchronize external clock input
When TCS = 0:
This bit is ignored. Read as '0'. Timer1 uses the internal clock when TCS = 0.
- bit 1 **TCS:** Timer Clock Sources Select bit
1 = External clock from pin TxCK
0 = Internal clock (Fosc/4)
- bit 0 **Unimplemented:** Read as '0'

Legend:
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR *1 = Bit is set *0 = Bit is cleared x = Bit is unknown



(a) Diagrama de conexión de los puertos B, C y D

(b) Registro de control del timer

TABLE 5-2: INTERRUPT CONTROLLER REGISTER MAP

| SFR Name | ADR | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset State |
|----------|------|--------|-------------|--------|--------|-------------|--------|--------|-------------|--------|-------|-------------|---------|---------|--------------|---------|---------------------|---------------------|
| INTCON1 | 0080 | NSTDIS | — | — | — | — | OVATE | OVBTE | COVTE | — | — | — | MATHERR | ADDRERR | STKERR | OSCFail | — | 0000 0000 0000 0000 |
| INTCON2 | 0082 | ALTIVT | — | — | — | — | — | — | — | — | — | — | INT4EP | INT3EP | INT2EP | INT1EP | INT0EP | 0000 0000 0000 0000 |
| IFS0 | 0084 | CNIF | M2CIF | SI2CIF | NVMIF | ADIF | U1TXIF | U1RXIF | SPI1IF | T3IF | T2IF | OC2IF | IC2IF | T1IF | OC1IF | IC1IF | INT0IF | 0000 0000 0000 0000 |
| IFS1 | 0086 | IC8IF | IC5IF | IC4IF | IC3IF | C1IF | SPI2IF | U2TXIF | U2RXIF | INT2IF | T5IF | T4IF | OC4IF | OC3IF | IC8IF | IC7IF | INT1IF | 0000 0000 0000 0000 |
| IFS2 | 0088 | — | — | — | FLTBIF | FLTAIF | LVDIF | — | QE1IF | PWMIF | C2IF | INT4IF | INT3IF | OC8IF | OC7IF | OC6IF | OC5IF | 0000 0000 0000 0000 |
| IEC0 | 008C | CNIE | M2CIE | SI2CIE | NVMIE | ADIE | U1TXIE | U1RXIE | SPI1IE | T3IE | T2IE | OC2IE | IC2IE | T1IE | OC1IE | IC1IE | INT0IE | 0000 0000 0000 0000 |
| IEC1 | 008E | IC8IE | IC5IE | IC4IE | IC3IE | C1IE | SPI2IE | U2TXIE | U2RXIE | INT2IE | T5IE | T4IE | OC4IE | OC3IE | IC8IE | IC7IE | INT1IE | 0000 0000 0000 0000 |
| IEC2 | 0090 | — | — | — | FLTBIE | FLTAIE | LVDIE | — | QE1IE | PWMIE | C2IE | INT4IE | INT3IE | OC8IE | OC7IE | OC6IE | OC5IE | 0000 0000 0000 0000 |
| IPC0 | 0094 | — | T1IP<2:0> | | — | OC1IP<2:0> | | — | IC1IP<2:0> | | — | INT0IP<2:0> | | — | INT0IP<2:0> | | 0100 0100 0100 0100 | |
| IPC1 | 0096 | — | T3IP<2:0> | | — | T2IP<2:0> | | — | OC2IP<2:0> | | — | IC2IP<2:0> | | — | IC2IP<2:0> | | 0100 0100 0100 0100 | |
| IPC2 | 0098 | — | ADIP<2:0> | | — | U1TXIP<2:0> | | — | U1RXIP<2:0> | | — | SPI1IP<2:0> | | — | SPI1IP<2:0> | | 0100 0100 0100 0100 | |
| IPC3 | 009A | — | CNIP<2:0> | | — | M2CIP<2:0> | | — | SI2CIP<2:0> | | — | NVMIP<2:0> | | — | NVMIP<2:0> | | 0100 0100 0100 0100 | |
| IPC4 | 009C | — | OC3IP<2:0> | | — | IC8IP<2:0> | | — | IC7IP<2:0> | | — | INT1IP<2:0> | | — | INT1IP<2:0> | | 0100 0100 0100 0100 | |
| IPC5 | 009E | — | INT2IP<2:0> | | — | T5IP<2:0> | | — | T4IP<2:0> | | — | OC4IP<2:0> | | — | OC4IP<2:0> | | 0100 0100 0100 0100 | |
| IPC6 | 00A0 | — | C1IP<2:0> | | — | SPI2IP<2:0> | | — | U2TXIP<2:0> | | — | U2RXIP<2:0> | | — | U2RXIP<2:0> | | 0100 0100 0100 0100 | |
| IPC7 | 00A2 | — | IC6IP<2:0> | | — | IC5IP<2:0> | | — | IC4IP<2:0> | | — | IC3IP<2:0> | | — | IC3IP<2:0> | | 0100 0100 0100 0100 | |
| IPC8 | 00A4 | — | OC8IP<2:0> | | — | OC7IP<2:0> | | — | OC6IP<2:0> | | — | OC5IP<2:0> | | — | OC5IP<2:0> | | 0100 0100 0100 0100 | |
| IPC9 | 00A6 | — | PWMIP<2:0> | | — | C2IP<2:0> | | — | INT4IP<2:0> | | — | INT3IP<2:0> | | — | INT3IP<2:0> | | 0100 0100 0100 0100 | |
| IPC10 | 00A8 | — | FLTAIP<2:0> | | — | LVDIP<2:0> | | — | — | | — | — | | — | QE1IP<2:0> | | 0100 0100 0000 0100 | |
| IPC11 | 00AA | — | — | — | — | — | — | — | — | — | — | — | — | — | FLTBIIP<2:0> | | 0000 0000 0000 0100 | |

Legend: u = uninitialized bit

Register 11-1: CNEN1: Input Change Notification Interrupt Enable Register1

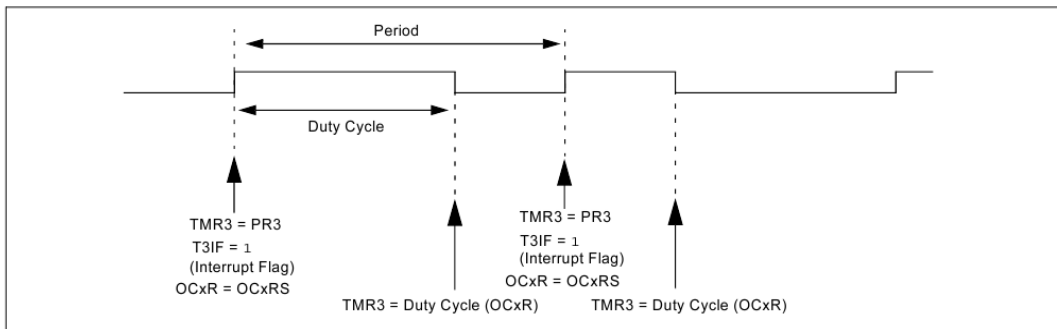
| Upper Byte: | | | | | | | |
|-------------|--------|--------|--------|--------|--------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CN15IE | CN14IE | CN13IE | CN12IE | CN11IE | CN10IE | CN9IE | CN8IE |
| bit 15 | | | | | | | bit 8 |

| Lower Byte: | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CN7IE | CN6IE | CN5IE | CN4IE | CN3IE | CN2IE | CN1IE | CN0IE |
| bit 7 | | | | | | | bit 0 |

bit 15-0 **CNxIE**: Input Change Notification Interrupt Enable bits

- 1 = Enable interrupt on input change
- 0 = Disable interrupt on input change

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset State |
|----------|-------|-------------------------------------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|--------|----------|-------|---------------------|---------------------|
| OC1RS | 0180 | Output Compare 1 Secondary Register | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| OC1R | 0182 | Output Compare 1 Main Register | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| OC1CON | 0184 | — | — | OCSIDL | — | — | — | — | — | — | — | — | OCFLT | OCTSEL | OCM<2:0> | | 0000 0000 0000 0000 | |
| OC2RS | 0186 | Output Compare 2 Secondary Register | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| OC2R | 0188 | Output Compare 2 Main Register | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| OC2CON | 018A | — | — | OCSIDL | — | — | — | — | — | — | — | — | OCFLT | OCTSE | OCM<2:0> | | 0000 0000 0000 0000 | |
| OC3RS | 018C | Output Compare 3 Secondary Register | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| OC3R | 018E | Output Compare 3 Main Register | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| OC3CON | 0190 | — | — | OCSIDL | — | — | — | — | — | — | — | — | OCFLT | OCTSEL | OCM<2:0> | | 0000 0000 0000 0000 | |
| OC4RS | 0192 | Output Compare 4 Secondary Register | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| OC4R | 0194 | Output Compare 4 Main Register | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| OC4CON | 0196 | — | — | OCSIDL | — | — | — | — | — | — | — | — | OCFLT | OCTSEL | OCM<2:0> | | 0000 0000 0000 0000 | |
| OC5RS | 0198 | Output Compare 5 Secondary Register | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| OC5R | 019A | Output Compare 5 Main Register | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| OC5CON | 019C | — | — | OCSIDL | — | — | — | — | — | — | — | — | OCFLT | OCTSEL | OCM<2:0> | | 0000 0000 0000 0000 | |
| OC6RS | 019E | Output Compare 6 Secondary Register | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| OC6R | 01A0 | Output Compare 6 Main Register | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| OC6CON | 01A2 | — | — | OCSIDL | — | — | — | — | — | — | — | — | OCFLT | OCTSEL | OCM<2:0> | | 0000 0000 0000 0000 | |
| OC7RS | 01A4 | Output Compare 7 Secondary Register | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| OC7R | 01A6 | Output Compare 7 Main Register | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| OC7CON | 01A8 | — | — | OCSIDL | — | — | — | — | — | — | — | — | OCFLT | OCTSEL | OCM<2:0> | | 0000 0000 0000 0000 | |
| OC8RS | 01AA | Output Compare 8 Secondary Register | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| OC8R | 01AC | Output Compare 8 Main Register | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |
| OC8CON | 01AE | — | — | OCSIDL | — | — | — | — | — | — | — | — | OCFLT | OCTSEL | OCM<2:0> | | 0000 0000 0000 0000 | |



Section 17. 10-bit A/D Converter

Register 17-1: ADCON1: A/D Control Register 1

| Upper Byte: | | | | | | | |
|-------------|-----|--------|-----|-----|-----|-----------|-------|
| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| ADON | — | ADSIDL | — | — | — | FORM<1:0> | bit 8 |

| Lower Byte: | | | | | | | |
|-------------|-------|--------|------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/C-0 |
| SSRC<2:0> | — | SIMSAM | ASAM | SAMP | DONE | | bit 0 |

- bit 15 **ADON:** A/D Operating Mode bit
1 = A/D converter module is operating
0 = A/D converter is off
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **ADSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters idle mode
0 = Continue module operation in idle mode
- bit 12-10 **Unimplemented:** Read as '0'
- bit 9-8 **FORM<1:0>:** Data Output Format bits
11 = Signed Fractional (DOU = dddd dddd dd00 0000)
10 = Fractional (DOU = dddd dddd dd00 0000)
01 = Signed Integer (DOU = xxxx xxxx dddd dddd)
00 = Integer (DOU = 0000 00dd dddd dddd)
- bit 7-5 **SSRC<2:0>:** Conversion Trigger Source Select bits
111 = Internal counter ends sampling and starts conversion (auto convert)
110 = Reserved
101 = Reserved
100 = Reserved
011 = Motor Control PWM interval ends sampling and starts conversion
010 = GP_Tmr3 compare ends sampling and starts conversion
001 = Active transition on INT0 pin ends sampling and starts conversion
000 = Clearing SAMP bit ends sampling and starts conversion
- bit 4 **Unimplemented:** Read as '0'
- bit 3 **SIMSAM:** Simultaneous Sample Select bit (only applicable when CHPS = 01 or 1x)
1 = Samples CH0, CH1, CH2, CH3 simultaneously (when CHPS = 1x)
or
Samples CH0 and CH1 simultaneously (when CHPS = 01)
0 = Samples multiple channels individually in sequence
- bit 2 **ASAM:** A/D Sample Auto-Start bit
1 = Sampling begins immediately after last conversion completes. SAMP bit is auto set
0 = Sampling begins when SAMP bit set
- bit 1 **SAMP:** A/D Sample Enable bit
1 = At least one A/D sample/hold amplifier is sampling
0 = A/D sample/hold amplifiers are holding
When ASAM = 0, writing '1' to this bit will start sampling
When SSRC = 000, writing '0' to this bit will end sampling and start conversion
- bit 0 **DONE:** A/D Conversion Status bit (Rev. B silicon or later)
1 = A/D conversion is done
0 = A/D conversion is NOT done
Cleared by software or start of a new conversion
Clearing this bit will not effect any operation in progress

Section 17. 10-bit A/D Converter

Register 17-2: ADCON2: A/D Control Register 2

| Upper Byte: | | | | | | | |
|-------------|----------|-----|-------|-----------|-------|-------|-------|
| R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| VCFG<2:0> | reserved | — | CSCNA | CHPS<1:0> | | | bit 8 |

| Lower Byte: | | | | | | | |
|-------------|-----|-----------|-------|-------|-------|-------|-------|
| R-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| BUFS | — | SMPI<3:0> | BUFM | ALTS | | | bit 0 |

- bit 15-13 **VCFG<2:0>:** Voltage Reference Configuration bits

| A/D VREFH | A/D VREFL |
|------------------------|--------------------|
| 000 AVDD | AVSS |
| 001 External VREF+ pin | AVSS |
| 010 AVDD | External VREF- pin |
| 011 External VREF+ pin | External VREF- pin |
| 100 AVDD | AVSS |
- bit 12 **Reserved:** User should write '0' to this location
- bit 11 **Unimplemented:** Read as '0'
- bit 10 **CSCNA:** Scan Input Selections for CH0+ S/H Input for MUX A Input Multiplexer Setting bit
1 = Scan inputs
0 = Do not scan inputs
- bit 9-8 **CHPS<1:0>:** Selects Channels Utilized bits
1x = Converts CH0, CH1, CH2 and CH3
01 = Converts CH0 and CH1
00 = Converts CH0
When SIMSAM bit (ADCON1<3>) = 0 multiple channels sampled sequentially
When SMSAM bit (ADCON1<3>) = 1 multiple channels sampled as in CHPS<1:0>
- bit 7 **BUFS:** Buffer Fill Status bit
Only valid when BUFM = 1 (ADRES split into 2 x 8-word buffers).
1 = A/D is currently filling buffer 0x8-0xF, user should access data in 0x0-0x7
0 = A/D is currently filling buffer 0x0-0x7, user should access data in 0x8-0xF
- bit 6 **Unimplemented:** Read as '0'
- bit 5-2 **SMPI<3:0>:** Sample/Convert Sequences Per Interrupt Selection bits
1111 = Interrupts at the completion of conversion for each 16th sample/convert sequence
1110 = Interrupts at the completion of conversion for each 15th sample/convert sequence
...
0001 = Interrupts at the completion of conversion for each 2nd sample/convert sequence
0000 = Interrupts at the completion of conversion for each sample/convert sequence
- bit 1 **BUFM:** Buffer Mode Select bit
1 = Buffer configured as two 8-word buffers ADCBUF(15..8), ADCBUF(7..0)
0 = Buffer configured as one 16-word buffer ADCBUF(15..0)
- bit 0 **ALTS:** Alternate Input Sample Mode Select bit
1 = Uses MUX A input multiplexer settings for first sample, then alternate between MUX B and MUX A input multiplexer settings for all subsequent samples
0 = Always use MUX A input multiplexer settings

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Register 17-3: ADCON3: A/D Control Register 3

| Upper Byte: | | | | | | | |
|-------------|-----|-----|-----------|-------|-------|-------|-------|
| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | — | — | SAMC<4:0> | | | | bit 8 |

| Lower Byte: | | | | | | | |
|-------------|-----|-----------|-------|-------|-------|-------|-------|
| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| ADRC | — | ADCS<5:0> | | | | | bit 0 |

- bit 15-13 **Unimplemented:** Read as '0'
- bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits
11111 = 31 TAD
...
00001 = 1 TAD
00000 = 0 TAD (only allowed if performing sequential conversions using more than one S/H amplifier)
- bit 7 **ADRC:** A/D Conversion Clock Source bit
1 = AD Internal RC clock
0 = Clock derived from system clock
- bit 6 **Unimplemented:** Read as '0'
- bit 5-0 **ADCS<5:0>:** A/D Conversion Clock Select bits
111111 = Tcv/2 + (ADCS<5:0> + 1) = 32 * Tcv
...
000001 = Tcv/2 + (ADCS<5:0> + 1) = Tcv
000000 = Tcv/2 + (ADCS<5:0> + 1) = Tcv/2

Legend:
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

Section 17. 10-bit A/D Converter

Register 17-4: ADCHS: A/D Input Select Register

| Upper Byte: | | | | | | | |
|--------------|---------|-------|------------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH123NB<1:0> | CH123SB | CH0NB | CH0SB<3:0> | | | | bit 8 |

| Lower Byte: | | | | | | | |
|--------------|---------|-------|------------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CH123NA<1:0> | CH123SA | CH0NA | CH0SA<3:0> | | | | bit 0 |

- bit 15-14 **CH123NB<1:0>:** Channel 1, 2, 3 Negative Input Select for MUX B Multiplexer Setting bits
Same definition as bits 6-7 (**Note**)
- bit 13 **CH123SB:** Channel 1, 2, 3 Positive Input Select for MUX B Multiplexer Setting bit
Same definition as bit 5 (**Note**)
- bit 12 **CH0NB:** Channel 0 Negative Input Select for MUX B Multiplexer Setting bit
Same definition as bit 4 (**Note**)
- bit 11-8 **CH0SB<3:0>:** Channel 0 Positive Input Select for MUX B Multiplexer Setting bits
Same definition as bits 3-0 (**Note**)
- bit 7-6 **CH123NA<1:0>:** Channel 1, 2, 3 Negative Input Select for MUX A Multiplexer Setting bits
11 = CH1 negative input is AN8, CH2 negative input is AN10, CH3 negative input is AN11
10 = CH1 negative input is AN6, CH2 negative input is AN7, CH3 negative input is AN8
0x = CH1, CH2, CH3 negative input is VREF-
- bit 5 **CH123SA:** Channel 1, 2, 3 Positive Input Select for MUX A Multiplexer Setting bit
1 = CH1 positive input is AN3, CH2 positive input is AN4, CH3 positive input is AN5
0 = CH1 positive input is AN0, CH2 positive input is AN1, CH3 positive input is AN2
- bit 4 **CH0NA:** Channel 0 Negative Input Select for MUX A Multiplexer Setting bit
1 = Channel 0 negative input is AN1
0 = Channel 0 negative input is VREF-
- bit 3-0 **CH0SA<3:0>:** Channel 0 Positive Input Select for MUX A Multiplexer Setting bits
1111 = Channel 0 positive input is AN15
1110 = Channel 0 positive input is AN14
1101 = Channel 0 positive input is AN13
||
||
0001 = Channel 0 positive input is AN1
0000 = Channel 0 positive input is AN0

Note: The analog input multiplexer supports two input setting configurations, denoted MUX A and MUX B. ADCHS<15:8> determine the settings for MUX B, and ADCHS<7:0> determine the settings for MUX A. Both sets of control bits function identically.

Note: The ADCHS register description and functionality will vary depending on the number of A/D inputs available on the selected device. Please refer to the specific device data sheet for additional details on this register.

Legend:
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown