15.0 MOTOR CONTROL PWM MODULE

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the *dsPIC30F Family Reference Manual* (DS70046).

This module simplifies the task of generating multiple, synchronized Pulse Width Modulated (PWM) outputs. In particular, the following power and motion control applications are supported by the PWM module:

- Three Phase AC Induction Motor
- Switched Reluctance (SR) Motor
- Brushless DC (BLDC) Motor
- Uninterruptible Power Supply (UPS)

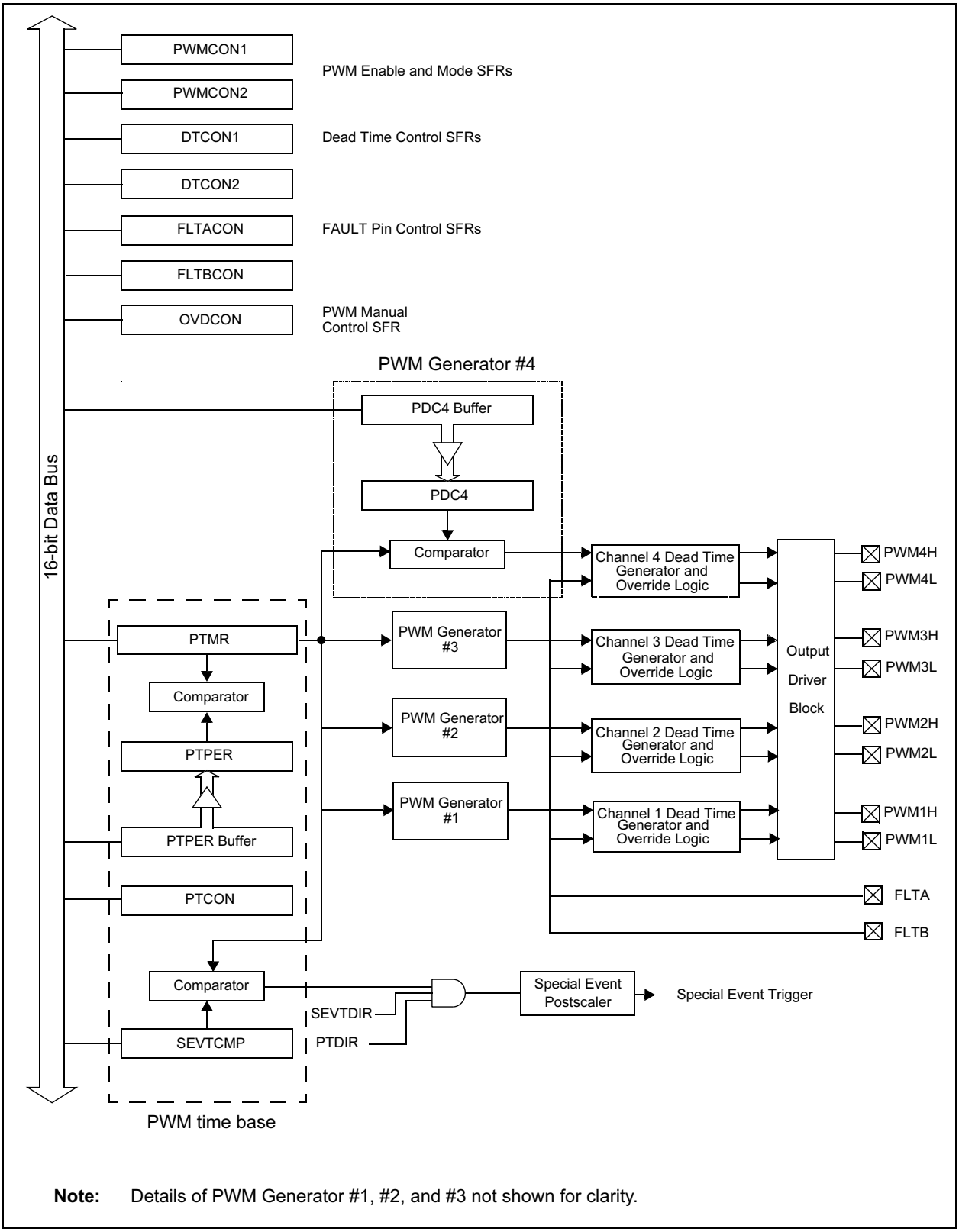
The PWM module has the following features:

- 8 PWM I/O pins with 4 duty cycle generators
- Up to 16-bit resolution
- 'On-the-Fly' PWM frequency changes
- Edge and Center Aligned Output modes
- Single Pulse Generation mode
- Interrupt support for asymmetrical updates in Center Aligned mode
- Output override control for Electrically Commutative Motor (ECM) operation
- 'Special Event' comparator for scheduling other peripheral events
- FAULT pins to optionally drive each of the PWM output pins to a defined state

This module contains 4 duty cycle generators, numbered 1 through 4. The module has 8 PWM output pins, numbered PWM1H/PWM1L through PWM4H/PWM4L. The eight I/O pins are grouped into high/low numbered pairs, denoted by the suffix H or L, respectively. For complementary loads, the low PWM pins are always the complement of the corresponding high I/O pin.

The PWM module allows several modes of operation which are beneficial for specific power control applications.

FIGURE 15-1: PWM MODULE BLOCK DIAGRAM



Note: Details of PWM Generator #1, #2, and #3 not shown for clarity.

15.1 PWM Time Base

The PWM time base is provided by a 15-bit timer with a prescaler and postscaler. The time base is accessible via the PTMR SFR. PTMR<15> is a Read Only Status bit, PTDIR, that indicates the present count direction of the PWM time base. If PTDIR is cleared, PTMR is counting upwards. If PTDIR is set, PTMR is counting downwards. The PWM time base is configured via the PTCON SFR. The time base is enabled/disabled by setting/clearing the PTEN bit in the PTCON SFR. PTMR is not cleared when the PTEN bit is cleared in software.

The PTPER SFR sets the counting period for PTMR. The user must write a 15-bit value to PTPER<14:0>. When the value in PTMR<14:0> matches the value in PTPER<14:0>, the time base will either reset to 0, or reverse the count direction on the next occurring clock cycle. The action taken depends on the operating mode of the time base.

Note:	If the period register is set to 0x0000, the timer will stop counting, and the interrupt and the special event trigger will not be generated, even if the special event value is also 0x0000. The module will not update the period register, if it is already at 0x0000; therefore, the user must disable the module in order to update the period register.

The PWM time base can be configured for four different modes of operation:

- Free Running mode
- Single Shot mode
- Continuous Up/Down Count mode
- Continuous Up/Down Count mode with interrupts for double updates

These four modes are selected by the PTMOD<1:0> bits in the PTCON SFR. The Up/Down Counting modes support center aligned PWM generation. The Single Shot mode allows the PWM module to support pulse control of certain Electronically Commutative Motors (ECMs).

The interrupt signals generated by the PWM time base depend on the mode selection bits (PTMOD<1:0>) and the postscaler bits (PTOPS<3:0>) in the PTCON SFR.

15.1.1 FREE RUNNING MODE

In the Free Running mode, the PWM time base counts upwards until the value in the Time Base Period register (PTPER) is matched. The PTMR register is reset on the following input clock edge and the time base will continue to count upwards as long as the PTEN bit remains set.

When the PWM time base is in the Free Running mode (PTMOD<1:0> = `00`), an interrupt event is generated each time a match with the PTPER register occurs and the PTMR register is reset to zero. The postscaler selection bits may be used in this mode of the timer to reduce the frequency of the interrupt events.

15.1.2 SINGLE SHOT MODE

In the Single Shot Counting mode, the PWM time base begins counting upwards when the PTEN bit is set. When the value in the PTMR register matches the PTPER register, the PTMR register will be reset on the following input clock edge and the PTEN bit will be cleared by the hardware to halt the time base.

When the PWM time base is in the Single Shot mode (PTMOD<1:0> = `01`), an interrupt event is generated when a match with the PTPER register occurs, the PTMR register is reset to zero on the following input clock edge, and the PTEN bit is cleared. The postscaler selection bits have no effect in this mode of the timer.

15.1.3 CONTINUOUS UP/DOWN COUNTING MODES

In the Continuous Up/Down Counting modes, the PWM time base counts upwards until the value in the PTPER register is matched. The timer will begin counting downwards on the following input clock edge. The PTDIR bit in the PTCON SFR is read only and indicates the counting direction The PTDIR bit is set when the timer counts downwards.

In the Up/Down Counting mode (PTMOD<1:0> = `10`), an interrupt event is generated each time the value of the PTMR register becomes zero and the PWM time base begins to count upwards. The postscaler selection bits may be used in this mode of the timer to reduce the frequency of the interrupt events.

15.1.4 DOUBLE UPDATE MODE

In the Double Update mode (PTMOD<1:0> = 11), an interrupt event is generated each time the PTMR register is equal to zero, as well as each time a period match occurs. The postscaler selection bits have no effect in this mode of the timer.

The Double Update mode provides two additional functions to the user. First, the control loop bandwidth is doubled because the PWM duty cycles can be updated, twice per period. Second, asymmetrical center-aligned PWM waveforms can be generated, which are useful for minimizing output waveform distortion in certain motor control applications.

Note:	Programming a value of 0x0001 in the period register could generate a continuous interrupt pulse, and hence, must be avoided.

15.1.5 PWM TIME BASE PRESCALER

The input clock to PTMR (FOSC/4), has prescaler options of 1:1, 1:4, 1:16, or 1:64, selected by control bits PTCKPS<1:0> in the PTCON SFR. The prescaler counter is cleared when any of the following occurs:

- a write to the PTMR register
- a write to the PTCON register
- any device Reset

The PTMR register is not cleared when PTCON is written.

15.1.6 PWM TIME BASE POSTSCALER

The match output of PTMR can optionally be postscaled through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling).

The postscaler counter is cleared when any of the following occurs:

- a write to the PTMR register
- a write to the PTCON register
- any device Reset

The PTMR register is not cleared when PTCON is written.

15.2 PWM Period

PTPER is a 15-bit register and is used to set the counting period for the PWM time base. PTPER is a double buffered register. The PTPER buffer contents are loaded into the PTPER register at the following instants:

- Free Running and Single Shot modes: When the PTMR register is reset to zero after a match with the PTPER register.
- Up/Down Counting modes: When the PTMR register is zero.

The value held in the PTPER buffer is automatically loaded into the PTPER register when the PWM time base is disabled (PTEN = 0).

The PWM period can be determined using Equation 15-1:

EQUATION 15-1: PWM PERIOD

$$T_{PWM} = \frac{T_{CY} \bullet (PTPER + 1)}{(\text{PTMR Prescale Value})}$$

If the PWM time base is configured for one of the Up/Down Count modes, the PWM period will be twice the value provided by Equation 15-1.

The maximum resolution (in bits) for a given device oscillator and PWM frequency can be determined using Equation 15-2:

EQUATION 15-2: PWM RESOLUTION

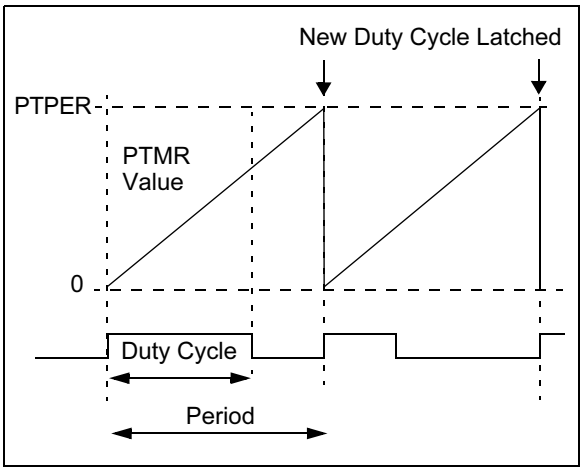
$$\text{Resolution} = \frac{\log (2 \bullet T_{PWM} / T_{CY})}{\log (2)}$$

15.3 Edge Aligned PWM

Edge aligned PWM signals are produced by the module when the PWM time base is in the Free Running or Single Shot mode. For edge aligned PWM outputs, the output has a period specified by the value in PTPER and a duty cycle specified by the appropriate duty cycle register (see Figure 15-2). The PWM output is driven active at the beginning of the period (PTMR = 0) and is driven inactive when the value in the duty cycle register matches PTMR.

If the value in a particular duty cycle register is zero, then the output on the corresponding PWM pin will be inactive for the entire PWM period. In addition, the output on the PWM pin will be active for the entire PWM period if the value in the duty cycle register is greater than the value held in the PTPER register.

FIGURE 15-2: EDGE ALIGNED PWM



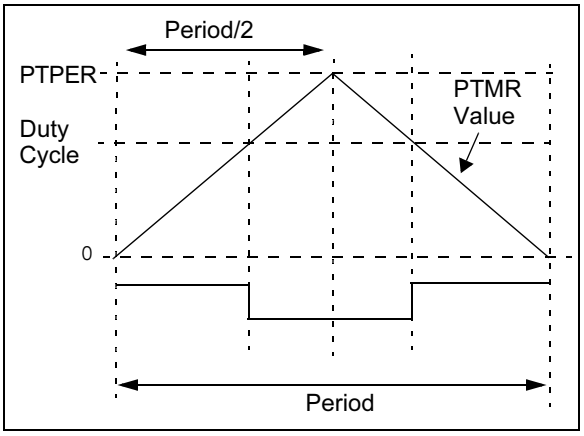
15.4 Center Aligned PWM

Center aligned PWM signals are produced by the module when the PWM time base is configured in an Up/Down Counting mode (see Figure 15-3).

The PWM compare output is driven to the active state when the value of the duty cycle register matches the value of PTMR and the PWM time base is counting downwards (PTDIR = 1). The PWM compare output is driven to the inactive state when the PWM time base is counting upwards (PTDIR = 0) and the value in the PTMR register matches the duty cycle value.

If the value in a particular duty cycle register is zero, then the output on the corresponding PWM pin will be inactive for the entire PWM period. In addition, the output on the PWM pin will be active for the entire PWM period if the value in the duty cycle register is equal to the value held in the PTPER register.

FIGURE 15-3: CENTER ALIGNED PWM



15.5 PWM Duty Cycle Comparison Units

There are four 16-bit special function registers (PDC1, PDC2, PDC3 and PDC4) used to specify duty cycle values for the PWM module.

The value in each duty cycle register determines the amount of time that the PWM output is in the active state. The duty cycle registers are 16-bits wide. The LS bit of a duty cycle register determines whether the PWM edge occurs in the beginning. Thus, the PWM resolution is effectively doubled.

15.5.1 DUTY CYCLE REGISTER BUFFERS

The four PWM duty cycle registers are double buffered to allow glitchless updates of the PWM outputs. For each duty cycle, there is a duty cycle register that is accessible by the user and a second duty cycle register that holds the actual compare value used in the present PWM period.

For edge aligned PWM output, a new duty cycle value will be updated whenever a match with the PTPER register occurs and PTMR is reset. The contents of the duty cycle buffers are automatically loaded into the duty cycle registers when the PWM time base is disabled (PTEN = 0) and the UDIS bit is cleared in PWMCON2.

When the PWM time base is in the Up/Down Counting mode, new duty cycle values are updated when the value of the PTMR register is zero and the PWM time base begins to count upwards. The contents of the duty cycle buffers are automatically loaded into the duty cycle registers when the PWM time base is disabled (PTEN = 0).

When the PWM time base is in the Up/Down Counting mode with double updates, new duty cycle values are updated when the value of the PTMR register is zero, and when the value of the PTMR register matches the value in the PTPER register. The contents of the duty cycle buffers are automatically loaded into the duty cycle registers when the PWM time base is disabled (PTEN = 0).

15.6 Complementary PWM Operation

In the Complementary mode of operation, each pair of PWM outputs is obtained by a complementary PWM signal. A dead time may be optionally inserted during device switching, when both outputs are inactive for a short period (Refer to Section 15.7).

In Complementary mode, the duty cycle comparison units are assigned to the PWM outputs as follows:

- PDC1 register controls PWM1H/PWM1L outputs
- PDC2 register controls PWM2H/PWM2L outputs
- PDC3 register controls PWM3H/PWM3L outputs
- PDC4 register controls PWM4H/PWM4L outputs

The Complementary mode is selected for each PWM I/O pin pair by clearing the appropriate PMODx bit in the PWMCON1 SFR. The PWM I/O pins are set to Complementary mode by default upon a device Reset.

15.7 Dead Time Generators

Dead time generation may be provided when any of the PWM I/O pin pairs are operating in the Complementary Output mode. The PWM outputs use Push-Pull drive circuits. Due to the inability of the power output devices to switch instantaneously, some amount of time must be provided between the turn off event of one PWM output in a complementary pair and the turn on event of the other transistor.

The PWM module allows two different dead times to be programmed. These two dead times may be used in one of two methods described below to increase user flexibility:

- The PWM output signals can be optimized for different turn off times in the high side and low side transistors in a complementary pair of transistors. The first dead time is inserted between the turn off event of the lower transistor of the complementary pair and the turn on event of the upper transistor. The second dead time is inserted between the turn off event of the upper transistor and the turn on event of the lower transistor.
- The two dead times can be assigned to individual PWM I/O pin pairs. This Operating mode allows the PWM module to drive different transistor/load combinations with each complementary PWM I/O pin pair.

15.7.1 DEAD TIME GENERATORS

Each complementary output pair for the PWM module has a 6-bit down counter that is used to produce the dead time insertion. As shown in Figure 15-4, each dead time unit has a rising and falling edge detector connected to the duty cycle comparison output.

15.7.2 DEAD TIME ASSIGNMENT

The DTCON2 SFR contains control bits that allow the dead times to be assigned to each of the complementary outputs. Table 15-1 summarizes the function of each dead time selection control bit.

TABLE 15-1: DEAD TIME SELECTION BITS

Bit	Function
DTS1A	Selects PWM1L/PWM1H active edge dead time.
DTS1I	Selects PWM1L/PWM1H inactive edge dead time.
DTS2A	Selects PWM2L/PWM2H active edge dead time.
DTS2I	Selects PWM2L/PWM2H inactive edge dead time.
DTS3A	Selects PWM3L/PWM3H active edge dead time.
DTS3I	Selects PWM3L/PWM3H inactive edge dead time.
DTS4A	Selects PWM4L/PWM4H active edge dead time.
DTS4I	Selects PWM4L/PWM4H inactive edge dead time.

15.7.3 DEAD TIME RANGES

The amount of dead time provided by each dead time unit is selected by specifying the input clock prescaler value and a 6-bit unsigned value. The amount of dead time provided by each unit may be set independently.

Four input clock prescaler selections have been provided to allow a suitable range of dead times, based on the device operating frequency. The clock prescaler option may be selected independently for each of the two dead time values. The dead time clock prescaler values are selected using the DTAPS<1:0> and DTBPS<1:0> control bits in the DTCON1 SFR. One of four clock prescaler options (T_{CY}, $2T_{CY}$, $4T_{CY}$ or $8T_{CY}$) may be selected for each of the dead time values.

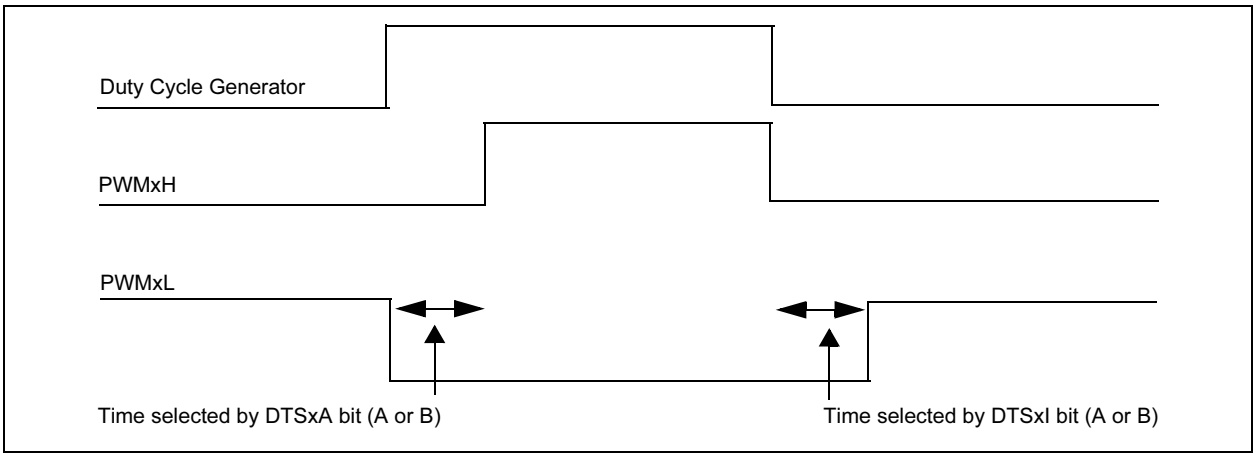
After the prescaler values are selected, the dead time for each unit is adjusted by loading two 6-bit unsigned values into the DTCON1 SFR.

The dead time unit prescalers are cleared on the following events:

- On a load of the down timer due to a duty cycle comparison edge event.
- On a write to the DTCON1 or DTCON2 registers.
- On any device Reset.

Note:	The user should not modify the DTCON1 or DTCON2 values while the PWM module is operating (PTEN = 1). Unexpected results may occur.

FIGURE 15-4: DEAD TIME TIMING DIAGRAM



15.8 Independent PWM Output

An independent PWM Output mode is required for driving certain types of loads. A particular PWM output pair is in the Independent Output mode when the corresponding PMOD bit in the PWMCON1 register is set. No dead time control is implemented between adjacent PWM I/O pins when the module is operating in the Independent mode and both I/O pins are allowed to be active simultaneously.

In the Independent mode, each duty cycle generator is connected to both of the PWM I/O pins in an output pair. By using the associated duty cycle register and the appropriate bits in the OVDCON register, the user may select the following signal output options for each PWM I/O pin operating in the Independent mode:

- I/O pin outputs PWM signal
- I/O pin inactive
- I/O pin active

15.9 Single Pulse PWM Operation

The PWM module produces single pulse outputs when the PTCON control bits PTMOD<1:0> = 10. Only edge aligned outputs may be produced in the Single Pulse mode. In Single Pulse mode, the PWM I/O pin(s) are driven to the active state when the PTEN bit is set. When a match with a duty cycle register occurs, the PWM I/O pin is driven to the inactive state. When a match with the PTPER register occurs, the PTMR register is cleared, all active PWM I/O pins are driven to the inactive state, the PTEN bit is cleared, and an interrupt is generated.

15.10 PWM Output Override

The PWM output override bits allow the user to manually drive the PWM I/O pins to specified logic states, independent of the duty cycle comparison units.

All control bits associated with the PWM output override function are contained in the OVDCON register. The upper half of the OVDCON register contains eight bits, POVDxH<4:1> and POVDxL<4:1>, that determine which PWM I/O pins will be overridden. The lower half of the OVDCON register contains eight bits, POUTxH<4:1> and POUTxL<4:1>, that determine the state of the PWM I/O pins when a particular output is overridden via the POVD bits.

15.10.1 COMPLEMENTARY OUTPUT MODE

When a PWMxL pin is driven active via the OVDCON register, the output signal is forced to be the complement of the corresponding PWMxH pin in the pair. Dead time insertion is still performed when PWM channels are overridden manually.

15.10.2 OVERRIDE SYNCHRONIZATION

If the OSYNC bit in the PWMCON2 register is set, all output overrides performed via the OVDCON register are synchronized to the PWM time base. Synchronous output overrides occur at the following times:

- Edge Aligned mode, when PTMR is zero.
- Center Aligned modes, when PTMR is zero and when the value of PTMR matches PTPER.

15.11 PWM Output and Polarity Control

There are three device configuration bits associated with the PWM module that provide PWM output pin control:

- HPOL configuration bit
- LPOL configuration bit
- PWMPIN configuration bit

These three bits in the FPORBOR configuration register (see Section 21) work in conjunction with the four PWM Enable bits (PWMEN<4:1>) located in the PWMCON1 SFR. The configuration bits and PWM Enable bits ensure that the PWM pins are in the correct states after a device Reset occurs. The PWMPIN configuration fuse allows the PWM module outputs to be optionally enabled on a device Reset. If PWMPIN = 0, the PWM outputs will be driven to their inactive states at Reset. If PWMPIN = 1 (default), the PWM outputs will be tri-stated. The HPOL bit specifies the polarity for the PWMxH outputs, whereas the LPOL bit specifies the polarity for the PWMxL outputs.

15.11.1 OUTPUT PIN CONTROL

The PEN<4:1>H and PEN<4:1>L control bits in the PWMCON1 SFR enable each high PWM output pin and each low PWM output pin, respectively. If a particular PWM output pin not enabled, it is treated as a general purpose I/O pin.

15.12 PWM FAULT Pins

There are two FAULT pins (FLTA and FLTB) associated with the PWM module. When asserted, these pins can optionally drive each of the PWM I/O pins to a defined state.

15.12.1 FAULT PIN ENABLE BITS

The FLTACON and FLTBCON SFRs each have 4 control bits that determine whether a particular pair of PWM I/O pins is to be controlled by the FAULT input pin. To enable a specific PWM I/O pin pair for FAULT overrides, the corresponding bit should be set in the FLTACON or FLTBCON register.

If all enable bits are cleared in the FLTACON or FLTBCON registers, then the corresponding FAULT input pin has no effect on the PWM module and the pin may be used as a general purpose interrupt or I/O pin.

Note:	The FAULT pin logic can operate independent of the PWM logic. If all the enable bits in the FLTACON/FLTBCON register are cleared, then the FAULT pin(s) could be used as general purpose interrupt pin(s). Each FAULT pin has an interrupt vector, Interrupt Flag bit and Interrupt Priority bits associated with it.

15.12.2 FAULT STATES

The FLTACON and FLTBCON special function registers have 8 bits each that determine the state of each PWM I/O pin when it is overridden by a FAULT input. When these bits are cleared, the PWM I/O pin is driven to the inactive state. If the bit is set, the PWM I/O pin will be driven to the active state. The active and inactive states are referenced to the polarity defined for each PWM I/O pin (HPOL and LPOL polarity control bits).

A special case exists when a PWM module I/O pair is in the Complementary mode and both pins are programmed to be active on a FAULT condition. The PWMxH pin always has priority in the Complementary mode, so that both I/O pins cannot be driven active simultaneously.

15.12.3 FAULT PIN PRIORITY

If both FAULT input pins have been assigned to control a particular PWM I/O pin, the FAULT state programmed for the FAULT A input pin will take priority over the FAULT B input pin.

15.12.4 FAULT INPUT MODES

Each of the FAULT input pins has two modes of operation:

- **Latched Mode:** When the FAULT pin is driven low, the PWM outputs will go to the states defined in the FLTACON/FLTBCON register. The PWM outputs will remain in this state until the FAULT pin is driven high and the corresponding interrupt flag has been cleared in software. When both of these actions have occurred, the PWM outputs will return to normal operation at the beginning of the next PWM cycle or half-cycle boundary. If the interrupt flag is cleared before the FAULT condition ends, the PWM module will wait until the FAULT pin is no longer asserted, to restore the outputs.
- **Cycle-by-Cycle Mode:** When the FAULT input pin is driven low, the PWM outputs remain in the defined FAULT states for as long as the FAULT pin is held low. After the FAULT pin is driven high, the PWM outputs return to normal operation at the beginning of the following PWM cycle or half-cycle boundary.

The Operating mode for each FAULT input pin is selected using the FLTAM and FLTBM control bits in the FLTACON and FLTBCON Special Function Registers.

Each of the FAULT pins can be controlled manually in software.

15.13 PWM Update Lockout

For a complex PWM application, the user may need to write up to four duty cycle registers and the time base period register, PTPER, at a given time. In some applications, it is important that all buffer registers be written before the new duty cycle and period values are loaded for use by the module.

The PWM update lockout feature is enabled by setting the UDIS control bit in the PWMCON2 SFR. The UDIS bit affects all duty cycle buffer registers and the PWM time base period buffer, PTPER. No duty cycle changes or period value changes will have effect while UDIS = 1.

15.14 PWM Special Event Trigger

The PWM module has a special event trigger that allows A/D conversions to be synchronized to the PWM time base. The A/D sampling and conversion time may be programmed to occur at any point within the PWM period. The special event trigger allows the user to minimize the delay between the time when A/D conversion results are acquired and the time when the duty cycle value is updated.

The PWM special event trigger has an SFR named SEVTCMP, and five control bits to control its operation. The PTMR value for which a special event trigger should occur is loaded into the SEVTCMP register. When the PWM time base is in an Up/Down Counting mode, an additional control bit is required to specify the counting phase for the special event trigger. The count phase is selected using the SEVTDIR control bit in the SEVTCMP SFR. If the SEVTDIR bit is cleared, the special event trigger will occur on the upward counting cycle of the PWM time base. If the SEVTDIR bit is set, the special event trigger will occur on the downward count cycle of the PWM time base. The SEVTDIR control bit has no effect unless the PWM time base is configured for an Up/Down Counting mode.

15.14.1 SPECIAL EVENT TRIGGER POSTSCALER

The PWM special event trigger has a postscaler that allows a 1:1 to 1:16 postscale ratio. The postscaler is configured by writing the SEVOPS<3:0> control bits in the PWMCON2 SFR.

The special event output postscaler is cleared on the following events:

- Any write to the SEVTCMP register
- Any device Reset

15.15 PWM Operation During CPU Sleep Mode

The FAULT A and FAULT B input pins have the ability to wake the CPU from Sleep mode. The PWM module generates an interrupt if either of the FAULT pins is driven low while in Sleep.

15.16 PWM Operation During CPU Idle Mode

The PTCON SFR contains a PTSIDL control bit. This bit determines if the PWM module will continue to operate or stop when the device enters Idle mode. If PTSIDL = 0, the module will continue to operate. If PTSIDL = 1, the module will stop operation as long as the CPU remains in Idle mode.

TABLE 15-2: 8-OUTPUT PWM REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
PTCON	01C0	PTEN	—	PTSIDL	—	—	—	—	—	PTOPS<3:0>				PTCKPS<1:0>		PTMOD<1:0>		0000 0000 0000 0000
PTMR	01C2	PTDIR	PWM Timer Count Value															0000 0000 0000 0000
PTPER	01C4	—	PWM Time Base Period Register															0000 0000 0000 0000
SEVTCMP	01C6	SEVTDIR	PWM Special Event Compare Register															0000 0000 0000 0000
PWMCON1	01C8	—	—	—	—	PTMOD4	PTMOD3	PTMOD2	PTMOD1	PEN4H	PEN3H	PEN2H	PEN1H	PEN4L	PEN3L	PEN2L	PEN1L	0000 0000 1111 1111
PWMCON2	01CA	—	—	—	—	SEVOPS<3:0>				—	—	—	—	—	—	OSYNC	UDIS	0000 0000 0000 0000
DTCON1	01CC	DTBPS<1:0>		Dead Time B Value						DTAPS<1:0>		Dead Time A Value						0000 0000 0000 0000
DTCON2	01CE	—	—	—	—	—	—	—	—	DTS4A	DTS4I	DTS3A	DTS3I	DTS2A	DTS2I	DTS1A	DTS1I	0000 0000 0000 0000
FLTACON	01D0	FAOV4H	FAOV4L	FAOV3H	FAOV3L	FAOV2H	FAOV2L	FAOV1H	FAOV1L	FLTAM	—	—	—	FAEN4	FAEN3	FAEN2	FAEN1	0000 0000 0000 0000
FLTBCON	01D2	FBOV4H	FBOV4L	FBOV3H	FBOV3L	FBOV2H	FBOV2L	FBOV1H	FBOV1L	FLTBM	—	—	—	FBEN4	FBEN3	FBEN2	FBEN1	0000 0000 0000 0000
OVDCON	01D4	POVD4H	POVD4L	POVD3H	POVD3L	POVD2H	POVD2L	POVD1H	POVD1L	POUT4H	POUT4L	POUT3H	POUT3L	POUT2H	POUT2L	POUT1H	POUT1L	1111 1111 0000 0000
PDC1	01D6	PWM Duty Cycle #1 Register																0000 0000 0000 0000
PDC2	01D8	PWM Duty Cycle #2 Register																0000 0000 0000 0000
PDC3	01DA	PWM Duty Cycle #3 Register																0000 0000 0000 0000
PDC4	01DC	PWM Duty Cycle #4 Register																0000 0000 0000 0000

Legend: u = uninitialized bit

Note: Refer to *dsPIC30F Family Reference Manual* (DS70046) for descriptions of register bit fields.

Section 15. Motor Control PWM

HIGHLIGHTS

This section of the manual contains the following topics:

15.1 Introduction

The motor control PWM (MCPWM) module simplifies the task of generating multiple, synchronized pulse width modulated outputs. In particular, the following power and motion control applications are supported:

- Three-Phase AC Induction Motor
- Switched Reluctance (SR) Motor
- Brushless DC (BLDC) Motor
- Uninterruptable Power Supply (UPS)

The PWM module has the following features:

- Dedicated time base supports TCY/2 PWM edge resolution
- Two output pins for each PWM generator
- Complementary or independent operation for each output pin pair
- Hardware dead time generators for complementary mode
- Output pin polarity programmed by device configuration bits
- Multiple output modes:
  - Edge aligned mode
  - Center aligned mode
  - Center aligned mode with double updates
  - Single event mode
- Manual override register for PWM output pins
- Duty cycle updates are configurable to be immediate or synchronized to the PWM
- Hardware fault input pins with programmable function
- Special Event Trigger for synchronizing A/D conversions
- Each output pin associated with the PWM can be individually enabled

15.1.1 MCPWM Module Variants

There are two versions of the MCPWM module depending on the dsPIC30F device that is selected. There is an 8-output module that is typically found on devices that have 64 or more pins. A 6-output MCPWM module is also available and is typically found on smaller devices that have less than 64 pins. A given dsPIC30F device may have more than one MCPWM module.

Please refer to the specific device data sheet for further details.

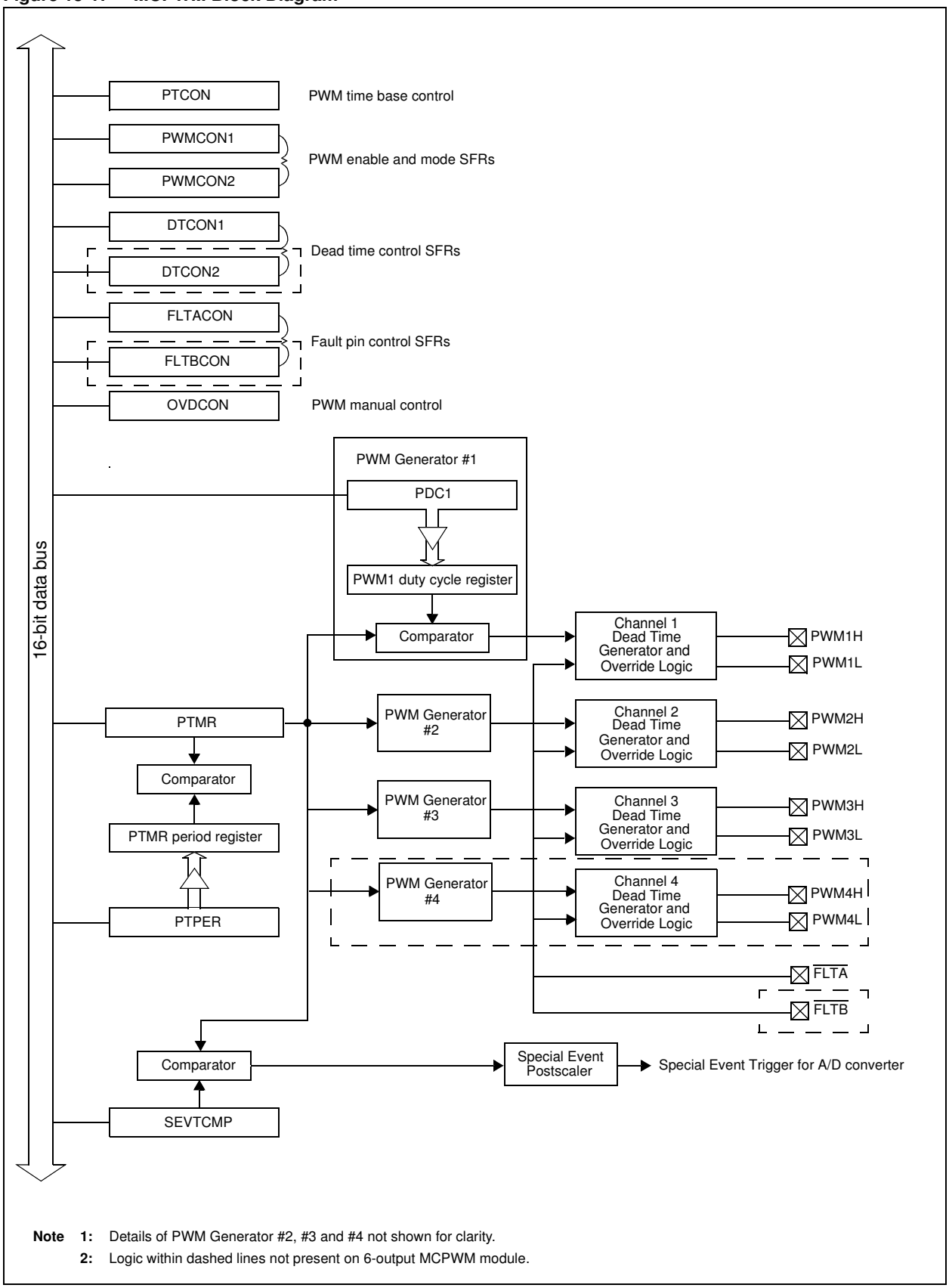
Table 15-1: Feature Summary: 6-Output MCPWM vs. 8-Output MCPWM

Feature	6-Output MCPWM Module	8-Output MCPWM Module
I/O Pins	6	8
PWM Generators	3	4
Fault Input Pins	1	2
Dead Time Generators	1	2

The 6-output MCPWM module is useful for single or 3-phase power application, while the 8 MCPWM can support 4-phase motor applications. Table 15-1 provides a feature summary for 6- and 8-output MCPWM modules. Both modules can support multiple single phase loads. The 8-output MCPWM also provides increased flexibility in an application because it supports two fault pins and two programmable dead times. These features are discussed in greater detail in subsequent sections.

A simplified block diagram of the MCPWM module is shown in Figure 15-1.

Figure 15-1: MCPWM Block Diagram



Note 1: Details of PWM Generator #2, #3 and #4 not shown for clarity.

2: Logic within dashed lines not present on 6-output MCPWM module.

15.2 Control Registers

The following registers control the operation of the MCPWM module:

- PTCON: PWM Time Base Control register
- PTMR: PWM Time Base register
- PTPER: PWM Time Base Period register
- SEVTCMP: PWM Special Event Compare register
- PWMCON1: PWM Control register #1
- PWMCON2: PWM Control register #2
- DTCON1: Dead Time Control register #1
- DTCON2: Dead Time Control register #2
- FLTACON: Fault A Control register
- FLTBCON: Fault B Control register
- PDC1: PWM Duty Cycle register #1
- PDC2: PWM Duty Cycle register #2
- PDC3: PWM Duty Cycle register #3
- PDC4: PWM Duty Cycle register #4

In addition, there are three device configuration bits associated with the MCPWM module to set up the initial Reset states and polarity of the I/O pins. These configuration bits are located in the FBORPOR device configuration register. Please refer to **Section 24. "Device Configuration"** for further details.

Register 15-1: PTCON: PWM Time Base Control Register

Upper Byte:							
R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
PTEN	—	PTSIDL	—	—	—	—	—
bit 15							bit 8

Lower Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTOPS<3:0>				PTCKPS<1:0>		PTMOD<1:0>	
bit 7							bit 0

bit 15 **PTEN:** PWM Time Base Timer Enable bit
1 = PWM time base is ON
0 = PWM time base is OFF

bit 14 **Unimplemented:** Read as '0'

bit 13 **PTSIDL:** PWM Time Base Stop in Idle Mode bit
1 = PWM time base halts in CPU Idle mode
0 = PWM time base runs in CPU Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7-4 **PTOPS<3:0>:** PWM Time Base Output Postscale Select bits
1111 = 1:16 Postscale
•
•
0001 = 1:2 Postscale
0000 = 1:1 Postscale

bit 3-2 **PTCKPS<1:0>:** PWM Time Base Input Clock Prescale Select bits
11 = PWM time base input clock period is 64 TCY (1:64 prescale)
10 = PWM time base input clock period is 16 TCY (1:16 prescale)
01 = PWM time base input clock period is 4 TCY (1:4 prescale)
00 = PWM time base input clock period is TCY (1:1 prescale)

bit 1-0 **PTMOD<1:0>:** PWM Time Base Mode Select bits
11 = PWM time base operates in a continuous up/down mode with interrupts for double PWM updates
10 = PWM time base operates in a continuous up/down counting mode
01 = PWM time base operates in single event mode
00 = PWM time base operates in a free running mode

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Register 15-2: PTMR: PWM Time Base Register

Upper Byte:							
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTDIR	PTMR <14:8>						
bit 15							bit 8

Lower Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTMR <7:0>							
bit 7							bit 0

bit 15 **PTDIR:** PWM Time Base Count Direction Status bit (Read Only)
1 = PWM time base is counting down
0 = PWM time base is counting up

bit 14-0 **PTMR <14:0>:** PWM Timebase Register Count Value

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Register 15-3: PTPER: PWM Time Base Period Register

Upper Byte:							
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PTPER <14:8>						
bit 15							bit 8

Lower Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTPER <7:0>							
bit 7							bit 0

bit 15 **Unimplemented:** Read as '0'

bit 14-0 **PTPER<14:0>:** PWM Time Base Period Value bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Register 15-4: SEVTCMP: Special Event Compare Register

Upper Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTDIR	SEVTCMP <14:8>						
bit 15							bit 8

Lower Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTCMP <7:0>							
bit 7							bit 0

bit 15 **SEVTDIR:** Special Event Trigger Time Base Direction bit(1)
1 = A special event trigger will occur when the PWM time base is counting downwards.
0 = A special event trigger will occur when the PWM time base is counting upwards.

bit 14-0 **SEVTCMP <14:0>:** Special Event Compare Value bit(2)

Note 1: SEVTDIR is compared with PTDIR (PTMR<15>) to generate the special event trigger.
2: SEVTCMP<14:0> is compared with PTMR<14:0> to generate the special event trigger.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Register 15-5: PWMCON1: PWM Control Register 1

Upper Byte:							
U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	PMOD4	PMOD3	PMOD2	PMOD1
bit 15							bit 8

Lower Byte:							
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
PEN4H	PEN3H	PEN2H	PEN1H	PEN4L	PEN3L	PEN2L	PEN1L
bit 7							bit 0

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **PMOD4:PMOD1:** PWM I/O Pair Mode bits
1 = PWM I/O pin pair is in the independent output mode
0 = PWM I/O pin pair is in the complementary output mode

bit 7-4 **PEN4H-PEN1H:** PWMxH I/O Enable bits(1)
1 = PWMxH pin is enabled for PWM output
0 = PWMxH pin disabled. I/O pin becomes general purpose I/O

bit 3-0 **PEN4L-PEN1L:** PWMxL I/O Enable bits(1)
1 = PWMxL pin is enabled for PWM output
0 = PWMxL pin disabled. I/O pin becomes general purpose I/O

Note 1: Reset condition of the PENxH and PENxL bits depend on the value of the PWM/PIN device configuration bit in the FBORPOR Device Configuration Register.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Register 15-6: PWMCON2: PWM Control Register 2

Upper Byte:							
U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	SEVOPS<3:0>			
bit 15							bit 8

Lower Byte:							
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	IUE	OSYNC	UDIS
bit 7							bit 0

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **SEVOPS<3:0>:** PWM Special Event Trigger Output Postscale Select bits
1111 = 1:16 Postscale
•
•
0001 = 1:2 Postscale
0000 = 1:1 Postscale

bit 7-2 **Unimplemented:** Read as '0'

bit 2 **IUE:** Immediate Update Enable bit(1)
1 = Updates to the active PDC registers are immediate
0 = Updates to the active PDC registers are synchronized to the PWM time base

bit 1 **OSYNC:** Output Override Synchronization bit
1 = Output overrides via the OVDCON register are synchronized to the PWM time base
0 = Output overrides via the OVDCON register occur on next TCY boundary

bit 0 **UDIS:** PWM Update Disable bit
1 = Updates from duty cycle and period buffer registers are disabled
0 = Updates from duty cycle and period buffer registers are enabled

Note 1: IUE bit is not implemented on the dsPIC30F6010 device.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Register 15-7: DTCON1: Dead Time Control Register 1

Upper Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTBPS<1:0>		DTB<5:0>					
bit 15							bit 8

Lower Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTAPS<1:0>		DTA<5:0>					
bit 7							bit 0

bit 15-14 **DTBPS<1:0>:** Dead Time Unit B Prescale Select bits
11 = Clock period for Dead Time Unit B is 8 TCY
10 = Clock period for Dead Time Unit B is 4 TCY
01 = Clock period for Dead Time Unit B is 2 TCY
00 = Clock period for Dead Time Unit B is TCY

bit 13-8 **DTB<5:0>:** Unsigned 6-bit Dead Time Value bits for Dead Time Unit B

bit 7-6 **DTAPS<1:0>:** Dead Time Unit A Prescale Select bits
11 = Clock period for Dead Time Unit A is 8 TCY
10 = Clock period for Dead Time Unit A is 4 TCY
01 = Clock period for Dead Time Unit A is 2 TCY
00 = Clock period for Dead Time Unit A is TCY

bit 5-0 **DTA<5:0>:** Unsigned 6-bit Dead Time Value bits for Dead Time Unit A

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Register 15-8: DTCON2: Dead Time Control Register 2

Upper Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

Lower Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTS4A	DTS4I	DTS3A	DTS3I	DTS2A	DTS2I	DTS1A	DTS1I
bit 7							bit 0

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **DTS4A:** Dead Time Select bit for PWM4 Signal Going Active
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

bit 6 **DTS4I:** Dead Time Select bit for PWM4 Signal Going Inactive
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

bit 5 **DTS3A:** Dead Time Select bit for PWM3 Signal Going Active
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

bit 4 **DTS3I:** Dead Time Select bit for PWM3 Signal Going Inactive
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

bit 3 **DTS2A:** Dead Time Select bit for PWM2 Signal Going Active
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

bit 2 **DTS2I:** Dead Time Select bit for PWM2 Signal Going Inactive
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

bit 1 **DTS1A:** Dead Time Select bit for PWM1 Signal Going Active
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

bit 0 **DTS1I:** Dead Time Select bit for PWM1 Signal Going Inactive
1 = Dead time provided from Unit B
0 = Dead time provided from Unit A

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Register 15-9: FLTACON: Fault A Control Register

Upper Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FAOV4H	FAOV4L	FAOV3H	FAOV3L	FAOV2H	FAOV2L	FAOV1H	FAOV1L
bit 15							bit 8

Lower Byte:							
R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTAM	—	—	—	FAEN4	FAEN3	FAEN2	FAEN1
bit 7							bit 0

bit 15-8 **FAOV4H-FAOV1L:** Fault Input A PWM Override Value bits
1 = The PWM output pin is driven ACTIVE on an external fault input event
0 = The PWM output pin is driven INACTIVE on an external fault input event

bit 7 **FLTAM:** Fault A Mode bit
1 = The Fault A input pin functions in the cycle-by-cycle mode
0 = The Fault A input pin latches all control pins to the programmed states in FLTACON<15:8>

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **FAEN4:** Fault Input A Enable bit
1 = PWM4H/PWM4L pin pair is controlled by Fault Input A
0 = PWM4H/PWM4L pin pair is not controlled by Fault Input A

bit 2 **FAEN3:** Fault Input A Enable bit
1 = PWM3H/PWM3L pin pair is controlled by Fault Input A
0 = PWM3H/PWM3L pin pair is not controlled by Fault Input A

bit 1 **FAEN2:** Fault Input A Enable bit
1 = PWM2H/PWM2L pin pair is controlled by Fault Input A
0 = PWM2H/PWM2L pin pair is not controlled by Fault Input A

bit 0 **FAEN1:** Fault Input A Enable bit
1 = PWM1H/PWM1L pin pair is controlled by Fault Input A
0 = PWM1H/PWM1L pin pair is not controlled by Fault Input A

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Register 15-10: FLTBCON: Fault B Control Register

Upper Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FBOV4H	FBOV4L	FBOV3H	FBOV3L	FBOV2H	FBOV2L	FBOV1H	FBOV1L
bit 15							bit 8

Lower Byte:							
R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTBM	—	—	—	FBEN4	FBEN3	FBEN2	FBEN1
bit 7							bit 0

bit 15-8 **FBOV4H:FBOV1L:** Fault Input B PWM Override Value bits
1 = The PWM output pin is driven ACTIVE on an external fault input event
0 = The PWM output pin is driven INACTIVE on an external fault input event

bit 7 **FLTBM:** Fault B Mode bit
1 = The Fault B input pin functions in the cycle-by-cycle mode
0 = The Fault B input pin latches all control pins to the programmed states in FLTBCON<15:8>

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **FAEN4:** Fault Input B Enable bit(1)
1 = PWM4H/PWM4L pin pair is controlled by Fault Input B
0 = PWM4H/PWM4L pin pair is not controlled by Fault Input B

bit 2 **FAEN3:** Fault Input B Enable bit(1)
1 = PWM3H/PWM3L pin pair is controlled by Fault Input B
0 = PWM3H/PWM3L pin pair is not controlled by Fault Input B

bit 1 **FAEN2:** Fault Input B Enable bit(1)
1 = PWM2H/PWM2L pin pair is controlled by Fault Input B
0 = PWM2H/PWM2L pin pair is not controlled by Fault Input B

bit 0 **FAEN1:** Fault Input B Enable bit(1)
1 = PWM1H/PWM1L pin pair is controlled by Fault Input B
0 = PWM1H/PWM1L pin pair is not controlled by Fault Input B

Note 1: Fault pin A has priority over Fault pin B, if enabled.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Register 15-11: OVDCON: Override Control Register

Upper Byte:							
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
POVD4H	POVD4L	POVD3H	POVD3L	POVD2H	POVD2L	POVD1H	POVD1L
bit 15							bit 8

Lower Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POUT4H	POUT4L	POUT3H	POUT3L	POUT2H	POUT2L	POUT1H	POUT1L
bit 7							bit 0

bit 15-8 **POVD4H-POVD1L:** PWM Output Override bits
1 = Output on PWMxx I/O pin is controlled by the PWM generator
0 = Output on PWMxx I/O pin is controlled by the value in the corresponding POUTxx bit

bit 7-0 **POUT4H-POUT1L:** PWM Manual Output bits
1 = PWMxx I/O pin is driven ACTIVE when the corresponding POVDxx bit is cleared
0 = PWMxx I/O pin is driven INACTIVE when the corresponding POVDxx bit is cleared

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Register 15-12: PDC1: PWM Duty Cycle Register 1

Upper Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWM Duty Cycle #1 bits 15-8							
bit 15							bit 8

Lower Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWM Duty Cycle #1 bits 7-0							
bit 7							bit 0

bit 15-0 **PDC1<15:0>:** PWM Duty Cycle #1 Value bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Register 15-13: PDC2: PWM Duty Cycle Register 2

Upper Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWM Duty Cycle #2 bits 15-8							
bit 15							bit 8

Lower Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWM Duty Cycle #2 bits 7-0							
bit 7							bit 0

bit 15-0 **PDC2<15:0>:** PWM Duty Cycle #2 Value bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Register 15-14: PDC3: PWM Duty Cycle Register 3

Upper Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWM Duty Cycle #3 bits 15-8							
bit 15							bit 8

Lower Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWM Duty Cycle #3 bits 7-0							
bit 7							bit 0

bit 15-0 **PDC3<15:0>:** PWM Duty Cycle #3 Value bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Register 15-15: PDC4: PWM Duty Cycle Register 4

Upper Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWM Duty Cycle #4 bits 15-8							
bit 15							bit 8

Lower Byte:							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWM Duty Cycle #4 bits 7-0							
bit 7							bit 0

bit 15-0 **PDC4<15:0>:** PWM Duty Cycle #4 Value bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Register 15-16: FBORPOR: BOR AND POR Device Configuration Register

Upper Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

Middle Byte:							
U-0	U-0	U-0	U-0	U-0	R/P	R/P	R/P
—	—	—	—	—	PWMPIN	HPOL	LPOL
bit 15							bit 8

Lower Byte:							
R/P	U-0	R/P	R/P	U-0	U-0	R/P	R/P
BOREN	—	BORV<1:0>		—	—	FPWRT<1:0>	
bit 7							bit 0

bit 10 **PWMPIN:** MPWM Drivers Initialization bit
1 = Pin state at reset controlled by I/O Port (PWMCON1<7:0> = 0x00)
0 = Pin state at reset controlled by module (PWMCON1<7:0> = 0xFF)

bit 9 **HPOL:** MCPWM High Side Drivers (PWMxH) Polarity bit
1 = Output signal on PWMxH pins has active high polarity
0 = Output signal on PWMxH pins has active low polarity

bit 8 **LPOL:** MCPWM Low Side Drivers (PWMxL) Polarity bit
1 = Output signal on PWMxL pins has active high polarity
0 = Output signal on PWMxL pins has active low polarity

Note: See **Section 24. "Device Configuration"** for information about other configuration bits on this register.

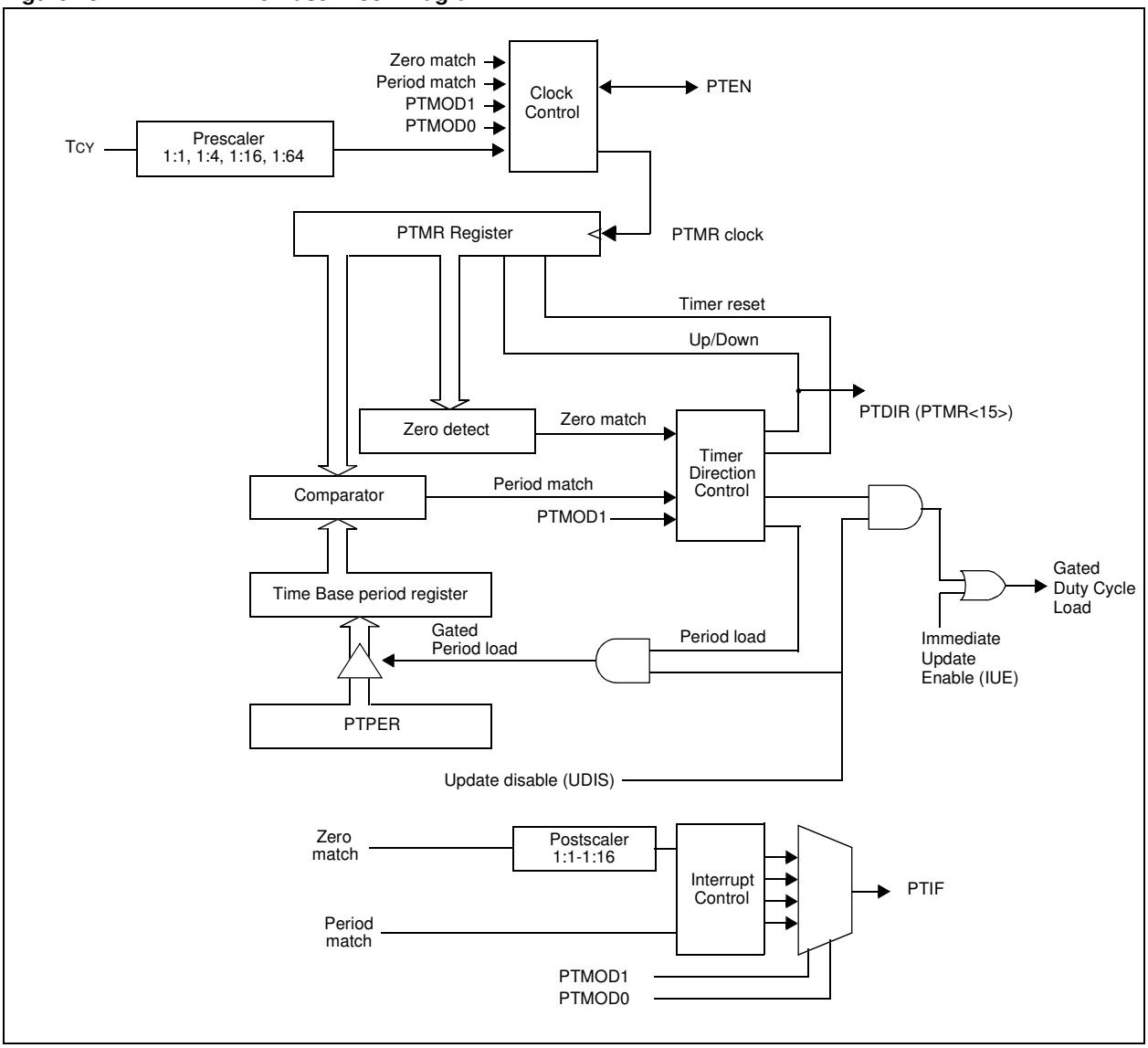
Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
P = Programmable configuration bit			

15.3 PWM Time Base

The PWM time base is provided by a 15-bit timer with a prescaler and postscaler (see Figure 15-2). The 15 bits of the time base are accessible via the PTMR register. PTMR<15> is a read-only status bit, PTDIR, that indicates the present count direction of the PWM time base. If the PTDIR status bit is cleared, PTMR is counting upwards. If PTDIR is set, PTMR is counting downwards.

The time base is enabled/disabled by setting/clearing the PTEN bit (PTCON<15>). PTMR is not cleared when the PTEN bit is cleared in software.

Figure 15-2: PWM Time Base Block Diagram



The PWM time base can be configured for four different modes of operation:

1. Free Running mode
2. Single Event mode
3. Continuous Up/Down Count mode
4. Continuous Up/Down Count mode with interrupts for double-updates.

These four modes are selected by the PTMOD<1:0> control bits (PTCON<1:0>).

Note:	The mode of the PWM time base determines the type of PWM signal that is generated by the module. (See Section 15.4.2, Section 15.4.3 and Section 15.4.4 for more details.)

15.3.1 Free Running Mode

In the Free Running mode, the time base will count upwards until the value in the PTPER register is matched. The PTMR register is reset on the following input clock edge and the time base will continue counting upwards as long as the PTEN bit remains set.

15.3.2 Single-Event Mode

In the Single Event Counting mode, the PWM time base will begin counting upwards when the PTEN bit is set. When the PTMR value matches the PTPER register, the PTMR register will be reset on the following input clock edge and the PTEN bit will be cleared by the hardware to halt the time base.

15.3.3 Up/Down Counting Modes

For the Continuous Up/Down Counting modes, the PWM time base will count upwards until the value in the PTPER register is matched. The timer will begin counting downwards on the following input clock edge and continue counting down until it reaches '0'. The PTDIR bit PTMR<15> is read-only and indicates the counting direction. The PTDIR bit is set when the timer counts downwards.

15.3.4 PWM Time Base Prescaler

The input clock to PTMR, (TCY) has prescaler options of 1:1, 1:4, 1:16 or 1:64 selected by control bits PTCKPS<1:0> (PTCON<3:2>). The prescaler counter is cleared when any of the following occurs:

- A write to the PTMR register
- A write to the PTCON register
- Any device reset

The PTMR register is not cleared when PTCON is written.

15.3.5 PWM Time Base Postscaler

The match output of PTMR can optionally be post-scaled through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling inclusive) to generate an interrupt. The postscaler is useful when the PWM duty cycle does not need to be updated every PWM cycle.

The postscaler counter is cleared when any of the following occurs:

- A write to the PTMR register
- A write to the PTCON register
- Any device reset

The PTMR register is not cleared when PTCON is written.

15.3.6 PWM Time Base Interrupts

The interrupt signals generated by the PWM time base depend on the mode selection bits, PTMOD<1:0> (PTCON<1:0>), and the time base postscaler bits, PTOPS<3:0> (PTCON<7:4>).

- **Free Running Mode**

When the PWM time base is in the Free Running mode (PTMOD<1:0> = 00), an interrupt is generated when the PTMR register is reset to '0', due to a match with the PTPER register. The postscaler selection bits may be used in this mode of the timer to reduce the frequency of the interrupt events.

- **Single Event Mode**

When the PWM time base is in the Single Event mode (PTMOD<1:0> = 01), an interrupt is generated when the PTMR register is reset to '0' due to a match with the PTPER register. The PTEN bit (PTCON<15>) is also cleared at this time to inhibit further PTMR increments. The postscaler selection bits have no effect in this mode of the timer.

- **Up/Down Counting Mode**

In the Up/Down Counting mode (PTMOD<1:0> = 10), an interrupt event is generated each time the value of the PTMR register becomes zero and the PWM time base begins to count upwards. The postscaler selection bits may be used in this mode of the timer to reduce the frequency of the interrupt events.

- **Up/Down Counting Mode with Double Updates**

In the Double Update mode (PTMOD<1:0> = 11), an interrupt event is generated each time the PTMR register is equal to zero and each time a period match occurs. The postscaler selection bits have no effect in this mode of the timer.

The Double Update mode allows the control loop bandwidth to be doubled because the PWM duty cycles can be updated twice per period. Every rising and falling edge of the PWM signal can be controlled using the double update mode.

15.3.7 PWM Period

The PTPER register sets the counting period for PTMR. The user must write a 15-bit value to PTPER<14:0>. When the value in PTMR<14:0> matches the value in PTPER<14:0>, the time base will either reset to '0' or reverse the count direction on the next clock input edge. The action taken depends on the operating mode of the time base.

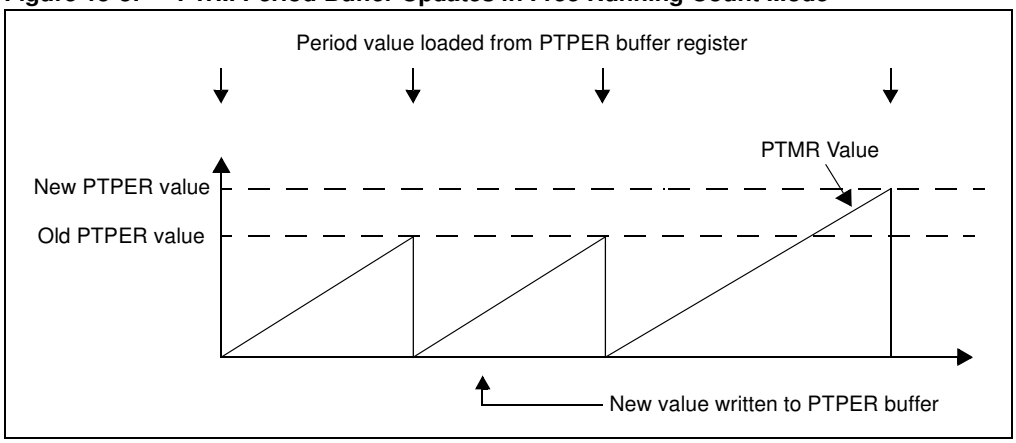
The time base period is double buffered to allow on-the-fly period changes of the PWM signal without glitches. The PTPER register serves as a buffer register to the actual time base period register, which is not accessible by the user. The PTPER register contents are loaded into the actual time base period register at the following times:

- Free Running and Single Event modes: when the PTMR register is reset to zero after a match with the PTPER register.
- Up/Down Counting modes: When the PTMR register is zero.

The value held in the PTPER register is automatically loaded into the time base period register when the PWM time base is disabled (PTEN = 0).

Figure 15-3 and Figure 15-4 indicate the times when the contents of the PTPER register are loaded into the time base period register.

Figure 15-3: PWM Period Buffer Updates in Free Running Count Mode



The PWM period can be determined from the following formula:

Equation 15-1: PWM Period Calculation for Free Running Count Mode (PTMOD = 10 or 11)

$$PTPER = \frac{F_{CY}}{F_{PWM} \bullet (PTMR\ Prescaler)} - 1$$

Example:

F_{CY} = 20 MHz

F_{PWM} = 20,000 Hz

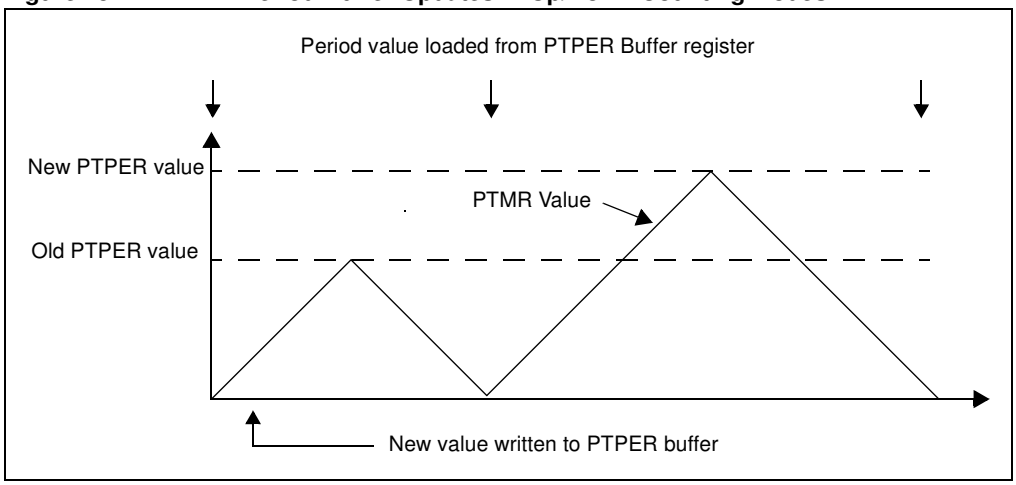
PTMR Prescaler = 1:1

$$PTPER = \frac{20{,}000{,}000}{20{,}000 \bullet 1} - 1$$

$$= 1000 - 1$$

$$= 999$$

Figure 15-4: PWM Period Buffer Updates in Up/Down Counting Modes



Equation 15-2: PWM Period Calculation in Up/Down Counting Modes (PTMOD = 00 or 01)

$$PTPER = \frac{FCY}{FPWM \bullet (PTMR\ Prescaler) \bullet 2} - 1$$

Example:

FCY = 20 MHz
FPWM = 20,000 Hz
PTMR Prescaler = 1:1

$$PTPER = \frac{20{,}000{,}000}{20{,}000 \bullet 1 \bullet 2} - 1$$

$$= 500 - 1$$
$$= 499$$

15.4 PWM Duty Cycle Comparison Units

The MCPWM module has four PWM generators. There are four 16-bit special function registers used to specify duty cycle values for the PWM generators:

- PDC1
- PDC2
- PDC3
- PDC4

In subsequent discussions, PDCx refers to any of the four PWM duty cycle registers.

15.4.1 PWM Duty Cycle Resolution

The maximum resolution (in bits) for a given device oscillator and PWM frequency can be determined from the following formula:

Equation 15-3: PWM Resolution

$$Resolution = \frac{\log\left(\frac{2T_{PWM}}{T_{CY}}\right)}{\log(2)}$$

The PWM resolutions and frequencies are shown in Table 15-2 for a selection of execution speeds and PTPER values. The PWM frequencies in Table 15-2 are for edge-aligned (Free Running PTMR) PWM mode. For center aligned modes (Up/Down PTMR mode), the PWM frequencies will be 1/2 the values as indicated in Table 15-3.

Table 15-2: Example PWM Frequencies and Resolutions, 1:1 Prescaler, Edge Aligned PWM

TCY (FCY)	PTPER Value	PDCx Value for 100%	PWM Resolution	PWM Frequency
33 ns (30 MHz)	0x7FFF	0xFFFF	16 bits	915 Hz
33 ns (30 MHz)	0x3FF	0x7FF	11 bits	29.3 kHz
50 ns (20 MHz)	0x7FFF	0xFFFF	16 bits	610 Hz
50 ns (20 MHz)	0x1FF	0x3FF	10 bits	39.1 kHz
100 ns (10 MHz)	0x7FFF	0xFFFF	16 bits	305 Hz
100 ns (10 MHz)	0xFF	0x1FF	9 bits	39.1 kHz
200 ns (5 MHz)	0x7FFF	0xFFFF	16 bits	153 Hz
200 ns (5 MHz)	0x7F	0xFF	8 bits	39.1 kHz

Table 15-3: Example PWM Frequencies and Resolutions, 1:1 Prescaler, Center Aligned PWM

TCY (FCY)	PTPER Value	PDCx Value for 100%	PWM Resolution	PWM Frequency
33 ns (30 MHz)	0x7FFF	0xFFFF	16 bits	458 Hz
33 ns (30 MHz)	0x3FFF	0x7FFF	15 bits	916 Hz
50 ns (20 MHz)	0x7FFF	0xFFFF	16 bits	305 Hz
50 ns (20 MHz)	0x1FFF	0x3FFF	14 bits	1.22 kHz
100 ns (10 MHz)	0x7FFF	0xFFFF	16 bits	153 Hz
100 ns (10 MHz)	0xFFF	0x1FFF	13 bits	1.22 kHz
200 ns (5 MHz)	0x7FFF	0xFFFF	16 bits	76.3 Hz
200 ns (5 MHz)	0x7FF	0xFFF	12 bits	1.22 kHz

The MCPWM module has the ability to produce PWM signal edges with TCY/2 resolution. PTMR increments every TCY with a 1:1 prescaler. To achieve TCY/2 edge resolution, PDCx<15:1> is compared to PTMR<14:0> to determine a duty cycle match. PDCx<0> determines whether the PWM signal edge will occur at the TCY or the TCY/2 boundary. When a 1:4, 1:16 or a 1:64 prescaler is used with the PWM time base, PDCx<0> is compared to the MSbit of the prescaler counter clock to determine when the PWM edge should occur.

PTMR and PDCx resolutions are depicted in Figure 15-5. It is shown that PTMR resolution is TCY and PDCx resolution is TCY/2 for 1:1 prescaler selection.

Figure 15-5: PTMR and PDCx Resolution Timing Diagram. Free Running Mode and 1:1 Prescaler Selection

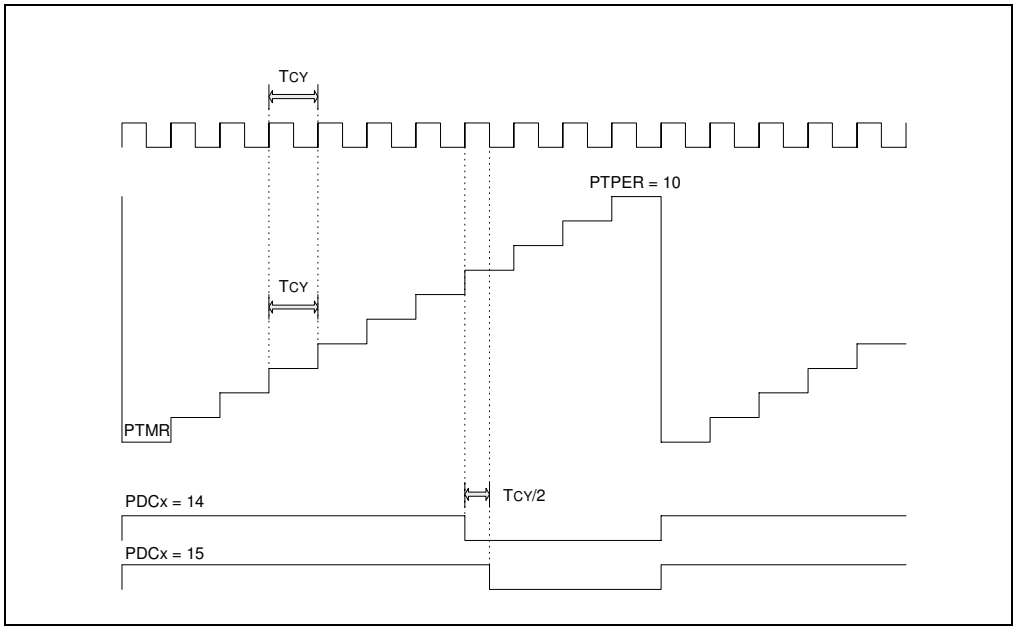
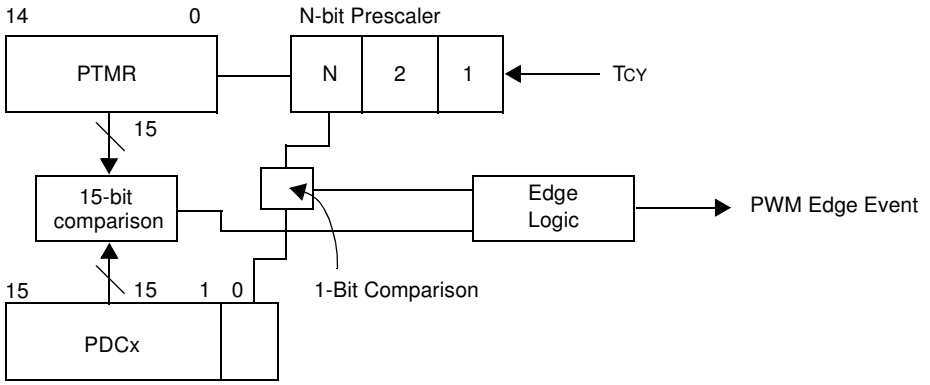


Figure 15-6: Duty Cycle Comparison Logic



Note: PDCx<0> is compared to the FOSC/2 signal when the prescaler is 1:1.

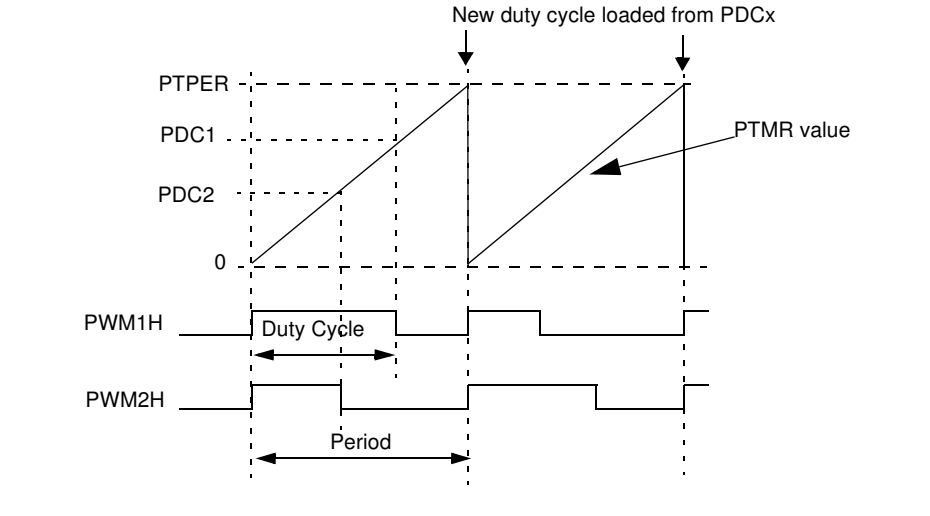
15.4.2 Edge Aligned PWM

Edge aligned PWM signals are produced by the module when the PWM time base is operating in the Free Running mode. The output signal for a given PWM channel has a period specified by the value loaded in PTPER and a duty cycle specified by the appropriate PDCx register (see Figure 15-7). Assuming a non-zero duty cycle and no immediate updates are enabled (IUE = 0), the outputs of all enabled PWM generators will be driven active at the beginning of the PWM period (PTMR = 0). Each PWM output will be driven inactive when the value of PTMR matches the duty cycle value of the PWM generator.

If the value in the PDCx register is zero, then the output on the corresponding PWM pin will be inactive for the entire PWM period. In addition, the output on the PWM pin will be active for the entire PWM period if the value in the PDCx register is greater than the value held in the PTPER register.

If immediate updates are enabled (IUE = 1), the new duty cycle value will be loaded at the time the new value is written to any active PDC register.

Figure 15-7: Edge-Aligned PWM

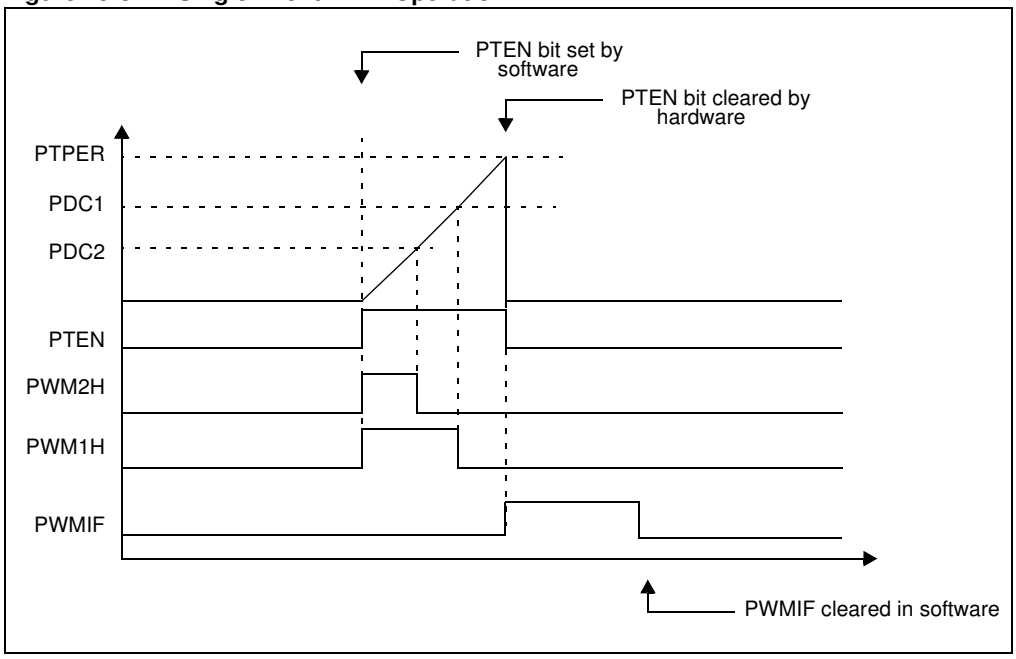


15.4.3 Single Event PWM Operation

The PWM module will produce single pulse outputs when the PWM time base is configured for the single event mode (PTMOD<1:0> = 01). This mode of operation is useful for driving certain types of electronically commutated motors. In particular, this mode is useful for high-speed SR motor operation. Only edge-aligned outputs may be produced in the Single Event mode.

In Single Event mode, the PWM I/O pin(s) are driven to the active state when the PTEN bit is set. When a match with a duty cycle register occurs, the PWM I/O pin is driven to the inactive state. When a match with the PTPER register occurs, the PTMR register is cleared, all active PWM I/O pins are driven to the inactive state, the PTEN bit is cleared, and an interrupt is generated. Operation of the PWM module will stop until the PTEN is set again in software.

Figure 15-8: Single Event PWM Operation



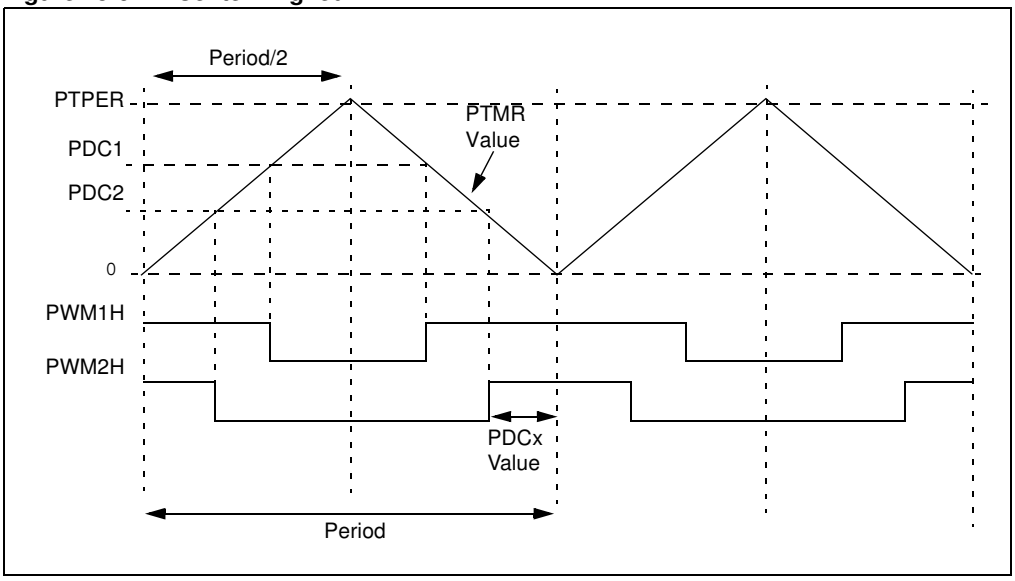
15.4.4 Center Aligned PWM

Center aligned PWM signals are produced by the module when the PWM time base is configured in one of the two Up/Down Counting modes (PTMOD<1:0> = 1x).

The PWM compare output is driven to the active state when the value of the Duty Cycle register matches the value of PTMR and the PWM time base is counting downwards (PTDIR = 1). The PWM compare output will be driven to the inactive state when the PWM time base is counting upwards (PTDIR = 0) and the value in the PTMR register matches the duty cycle value.

If the value in a particular Duty Cycle register is zero, then the output on the corresponding PWM pin will be inactive for the entire PWM period. In addition, the output on the PWM pin will be active for the entire PWM period if the value in the Duty Cycle register is greater than the value held in the PTPER register.

Figure 15-9: Center Aligned PWM



15.4.5 Duty Cycle Register Buffering

The four PWM duty cycle registers, PDC1-PDC4, are buffered to allow glitchless updates of the PWM outputs. For each generator, there is the PDCx register (buffer register) that is accessible by the user and the non-memory mapped Duty Cycle register that holds the actual compare value. The PWM duty cycle is updated with the value in the PDCx register at specific times in the PWM period to avoid glitches in the PWM output signal.

When the PWM time base is operating in the Free Running or Single Event modes (PTMOD<1:0> = 0x), the PWM duty cycle is updated whenever a match with the PTPER register occurs and PTMR is reset to '0'.

Note:	Any write to the PDCx registers will immediately update the duty cycle when the PWM time base is disabled (PTEN = 0). This allows a duty cycle change to take effect before PWM signal generation is enabled.

When the PWM time base is operating in the Up/Down Counting mode (PTMOD<1:0> = 10), duty cycles are updated when the value of the PTMR register is zero and the PWM time base begins to count upwards. Figure 15-10 indicates the times when the duty cycle updates occur for this mode of the PWM time base.

When the PWM time base is in the Up/Down Counting mode with double updates (PTMOD<1:0> = 11), duty cycles are updated when the value of the PTMR register is zero and when the value of the PTMR register matches the value in the PTPER register. Figure 15-11 indicates the times when the duty cycle updates occur for this mode of the PWM time base.

Figure 15-10: Duty Cycle Update Times in Up/Down Count Mode

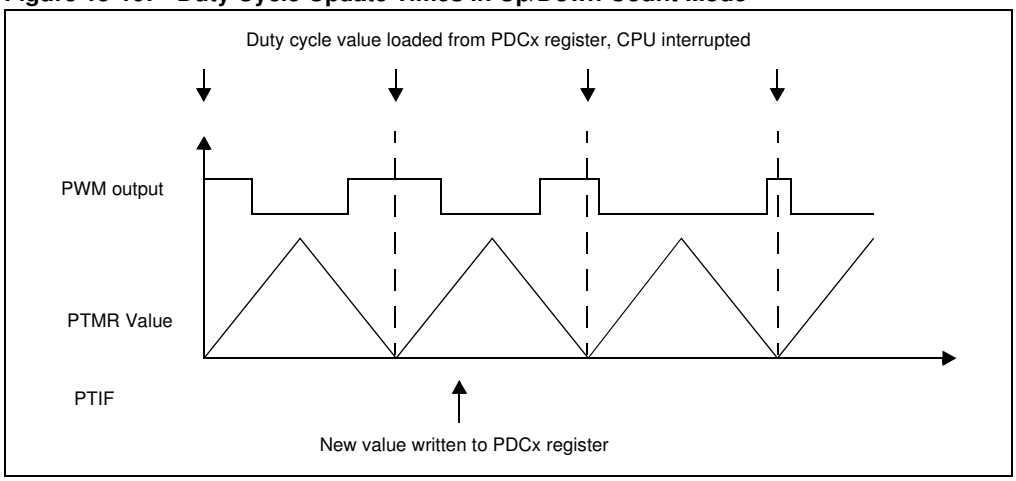
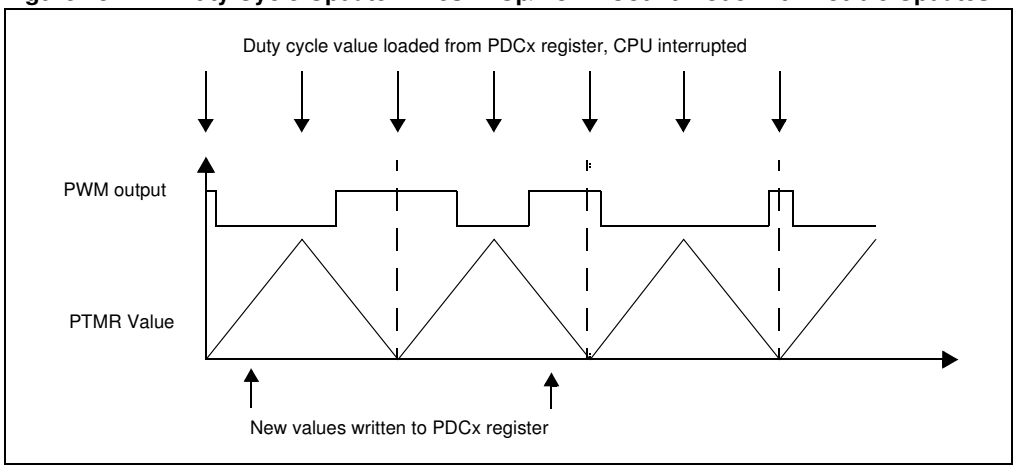


Figure 15-11: Duty Cycle Update Times in Up/Down Count Mode with Double Updates



15.4.6 PWM Duty Cycle Immediate Updates

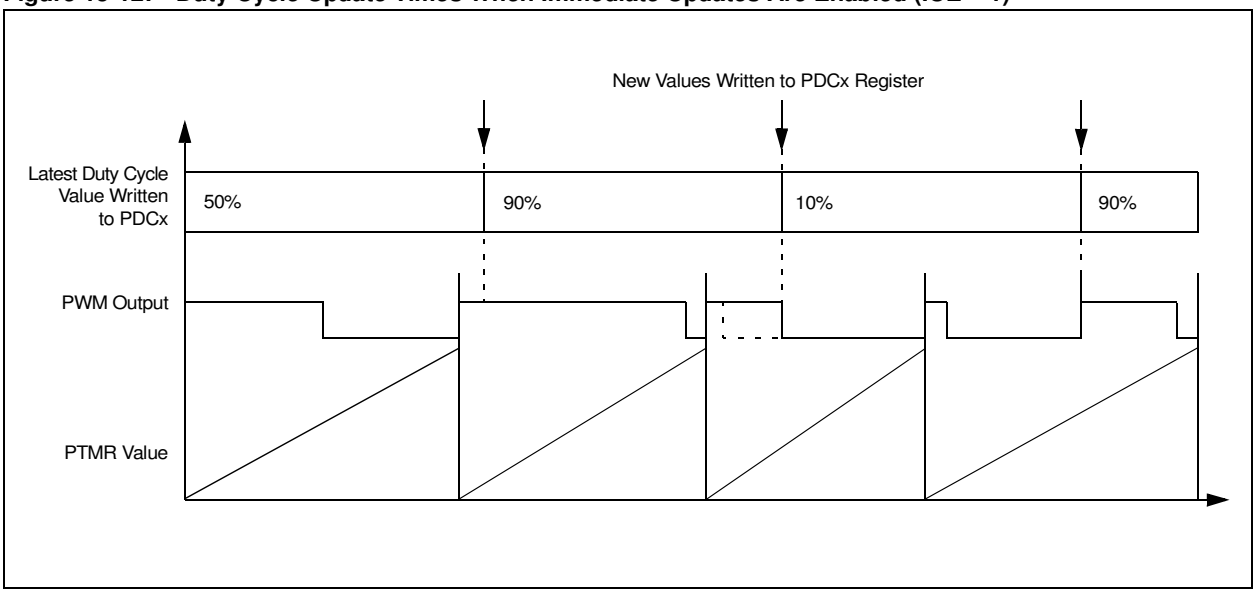
When the Immediate Update Enable bit is set (IUE = 1), any write to the duty cycle registers will update the new duty cycle value immediately. This feature gives the option to the user to allow immediate updates of the active PWM duty cycle registers instead of waiting for the end of the current time base period. System stability is improved in closed loop servo applications by reducing the delay between system observation and the issuance of system corrective commands when immediate updates are enabled (IUE = 1).

If the PWM output is active at the time the new duty cycle is written and the new duty cycle is less than the current time base value, the PWM pulse width will be shortened. If the PWM output is active at the time the new duty cycle is written and the new duty cycle is greater than the current time base value, the PWM pulse width will be lengthened. If the PWM output is inactive at the time the new duty cycle is written and the new duty cycle is greater than the current time base value, the PWM output will become active immediately and will remain active for the new written duty cycle value.

Figure 15-12 indicates the times when the duty cycle updates occur when immediate updates are enabled (IUE = 1)..

Note:	The IUE bit is not implemented on the dsPIC30F6010 device.

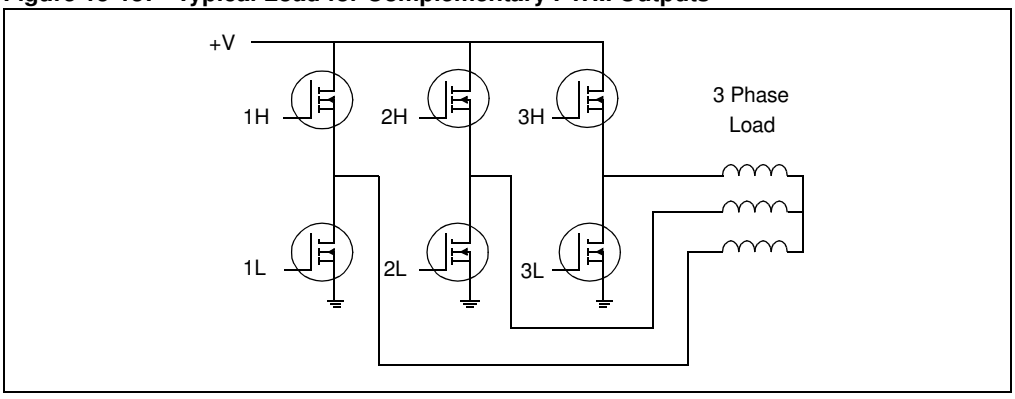
Figure 15-12: Duty Cycle Update Times When Immediate Updates Are Enabled (IUE = 1)



15.5 Complementary PWM Output Mode

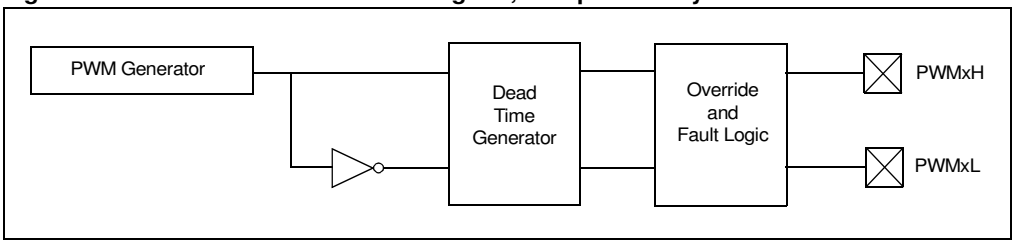
The Complementary Output mode is used to drive inverter loads similar to the one shown in Figure 15-13. This inverter topology is typical for ACIM and BLDC applications. In the Complementary Output mode, a pair of PWM outputs cannot be active simultaneously. Each PWM channel and output pin pair is internally configured as shown in Figure 15-14. A dead time may be optionally inserted during device switching where both outputs are inactive for a short period (Refer to **Section 15.6 "Dead Time Control"**).

Figure 15-13: Typical Load for Complementary PWM Outputs



The Complementary mode is selected for each PWM I/O pin pair by clearing the appropriate PMODx bit in PWMCON1. The PWM I/O pins are set to complementary mode by default upon a device reset.

Figure 15-14: PWM Channel Block Diagram, Complementary Mode



15.6 Dead Time Control

Dead time generation is automatically enabled when any of the PWM I/O pin pairs are operating in the Complementary Output mode. Because the power output devices cannot switch instantaneously, some amount of time must be provided between the turn-off event of one PWM output in a complementary pair and the turn-on event of the other transistor.

The 6-output PWM module has one programmable dead time. The 8-output PWM module allows two different dead times to be programmed. These two dead times may be used in one of two methods described below to increase user flexibility:

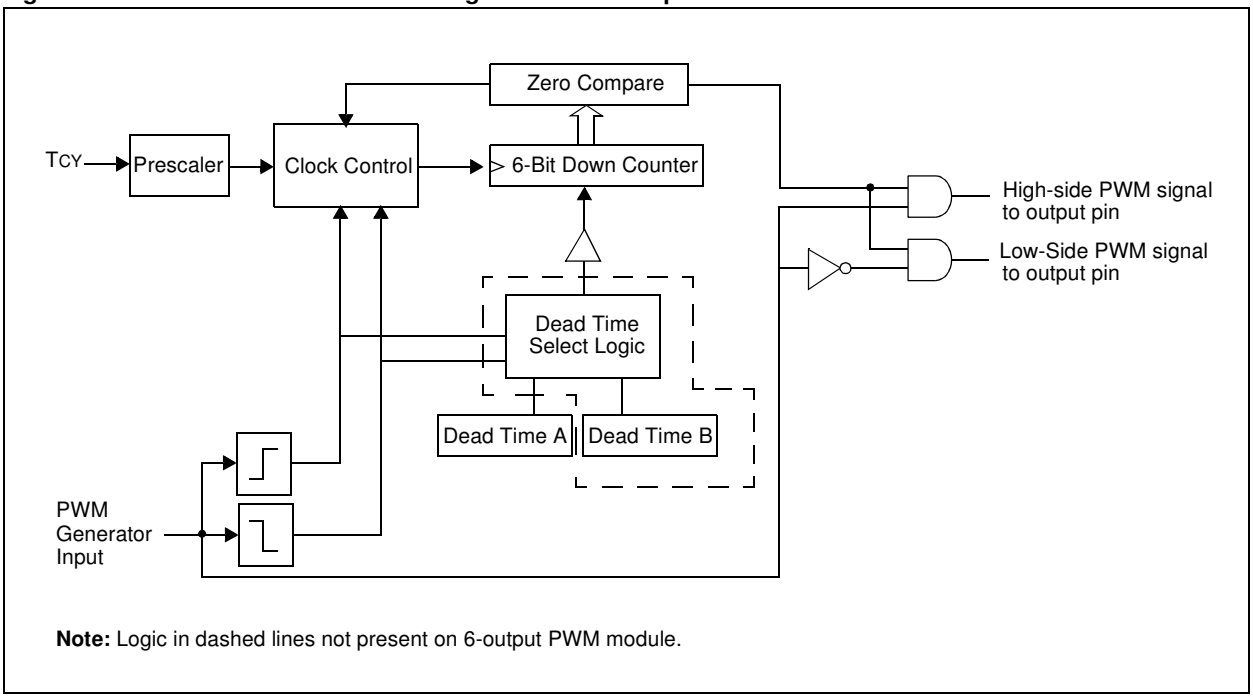
- The PWM output signals can be optimized for different turn-off times in the high-side and low-side transistors. The first dead time is inserted between the turn-off event of the lower transistor of the complementary pair and the turn-on event of the upper transistor. The second dead time is inserted between the turn-off event of the upper transistor and the turn-on event of the lower transistor.
- The two dead times can be assigned to individual PWM I/O pin pairs. This operating mode allows the PWM module to drive different transistor/load combinations with each complementary PWM I/O pin pair.

15.6.1 Dead Time Generators

Each complementary output pair for the PWM module has a 6-bit down counter that is used to produce the dead time insertion. As shown in Figure 15-15, each dead time unit has a rising and falling edge detector connected to the duty cycle comparison output.

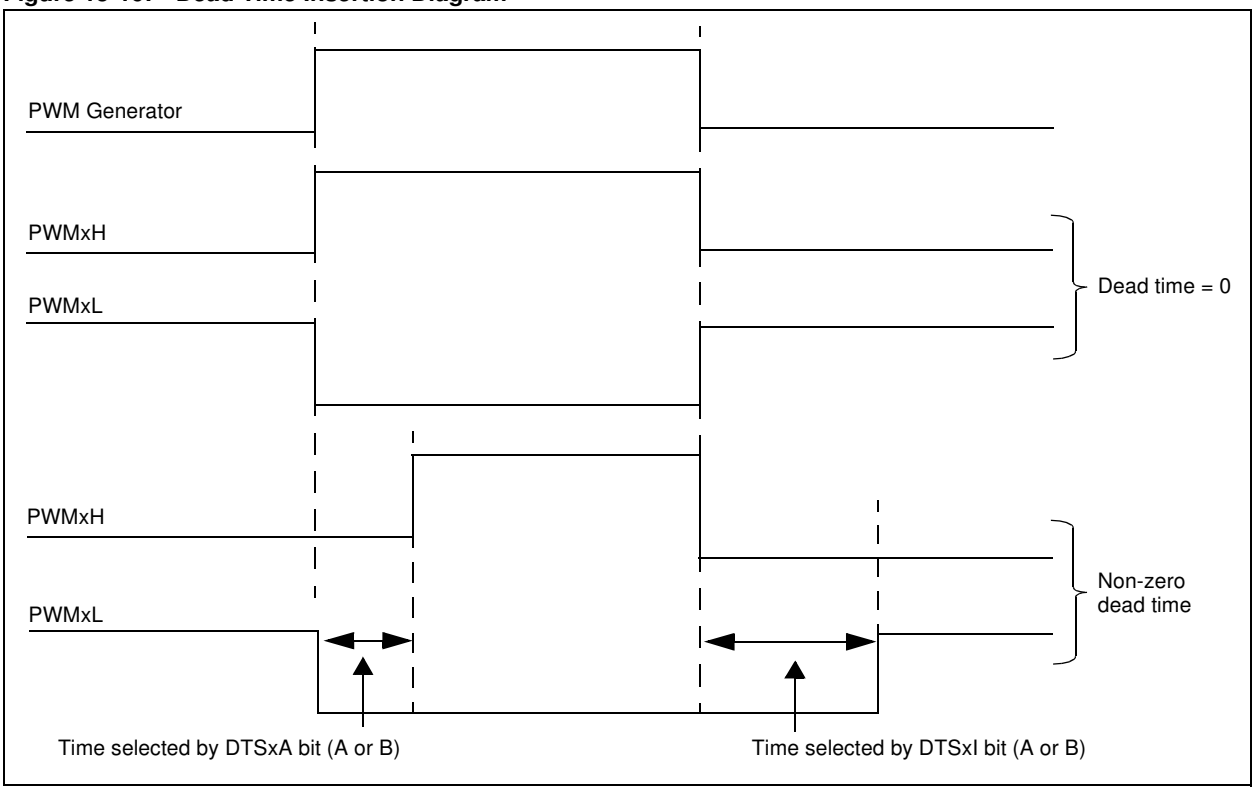
One of the two possible dead times is loaded into the timer on the detected PWM edge event. Depending on whether the edge is rising or falling, one of the transitions on the complementary outputs is delayed until the timer counts down to zero. A timing diagram indicating the dead time insertion for one pair of PWM outputs is shown in Figure 15-16. The use of two different dead times for the rising and falling edge events has been exaggerated in the figure for clarity.

Figure 15-15: Dead Time Unit Block Diagram for One Output Pin Pair



Note: Logic in dashed lines not present on 6-output PWM module.

Figure 15-16: Dead Time Insertion Diagram



15.6.2 Dead Time Assignment

Note: The dead time assignment logic is only applicable to dsPIC variants that contain the 8-output PWM module. The 6-output PWM module uses dead time A only.

The DTCON2 register contains control bits that allow the two programmable dead times to be assigned to each of the complementary outputs. There are two dead time assignment control bits for each of the complementary outputs. For example, the DTS1A and DTS1I control bits select the dead times to be used for the PWM1H/PWM1L complementary output pair. The pair of dead time selection control bits are referred to as the 'dead-time-select-active' and 'dead-time-select-inactive' control bits, respectively. The function of each bit in a pair is as follows:

- The DTSxA control bit selects the dead time that is to be inserted before the high-side output is driven active.
- The DTSxI control bit selects the dead time that is to be inserted before the low-side PWM active is driven active.

Table 15-4 summarizes the function of each dead time selection control bit.

Table 15-4: Dead Time Selection Bits

Bit	Function
DTS1A	Selects PWM1H/PWM1L dead time inserted before PWM1H is driven active.
DTS1I	Selects PWM1H/PWM1L dead time inserted before PWM1L is driven active.
DTS2A	Selects PWM1H/PWM1L dead time inserted before PWM2H is driven active.
DTS2I	Selects PWM1H/PWM1L dead time inserted before PWM2L is driven active.
DTS3A	Selects PWM1H/PWM1L dead time inserted before PWM3H is driven active.
DTS3I	Selects PWM1H/PWM1L dead time inserted before PWM3L is driven active.
DTS4A	Selects PWM1H/PWM1L dead time inserted before PWM4H is driven active.
DTS4I	Selects PWM1H/PWM1L dead time inserted before PWM4L is driven active.

15.6.3 Dead Time Ranges

Dead time A and dead time B are set by selecting an input clock prescaler value and a 6-bit unsigned dead time count value.

Four input clock prescaler selections have been provided to allow a suitable range of dead times based on the device operating frequency. The clock prescaler option may be selected independently for each of the two dead time values. The dead time clock prescaler values are selected using the DTAPS<1:0> and DTBPS<1:0> control bits in the DTCON1 SFR. The following clock prescaler options may be selected for each of the dead time values:

- T_{CY}
- 2 T_{CY}
- 4 T_{CY}
- 8 T_{CY}

Equation 15-4: Dead Time Calculation

$$DT = \frac{\text{Dead Time}}{\text{Prescale Value} \bullet T_{CY}}$$

Note: DT (Dead Time) is the DTA<5:0> or DTB<5:0> register value.

Table 15-5 shows example dead time ranges as a function of the input clock prescaler selected and the device operating frequency.

Table 15-5: Example Dead Time Ranges

TCY (FCY)	Prescaler Selection	Resolution	Dead Time Range
33 ns (30 MHz)	4 TCY	130 ns	130 ns -9 µs
50 ns (20 MHz)	4 TCY	200 ns	200 ns -12 µs
100 ns (10 MHz)	2 TCY	200 ns	200 ns -12 µs
100 ns (10 MHz)	1 TCY	100 ns	100 ns - 6 µs

15.6.4 Dead Time Distortion

For small PWM duty cycles, the ratio of dead time to the active PWM time may become large. At the extreme case, when the duty cycle is less than or equal to the programmed duty cycle, no PWM pulse will be generated. In these cases, the inserted dead time will introduce distortion into waveforms produced by the PWM module. The user can ensure that dead time distortion is minimized by keeping the PWM duty cycle at least three times larger than the dead time. Dead time distortion can also be corrected by other techniques, such as closed loop current control.

A similar effect occurs for duty cycles near 100%. The maximum duty cycle used in the application should be chosen such that the minimum inactive time of the PWM signal is at least three times larger than the dead time.

15.7 Independent PWM Output Mode

An Independent PWM Output mode is useful for driving loads such as the one shown in Figure 15-17. A particular PWM output pair is in the Independent Output mode when the corresponding PMOD bit in the PWMCON1 register is set. The dead time generators are disabled in the Independent mode and there are no restrictions on the state of the pins for a given output pin pair.

Figure 15-17: Asymmetric Inverter

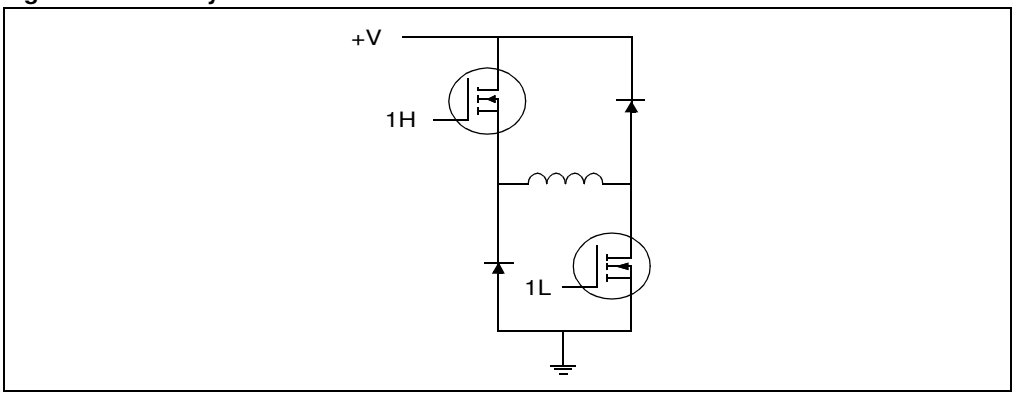
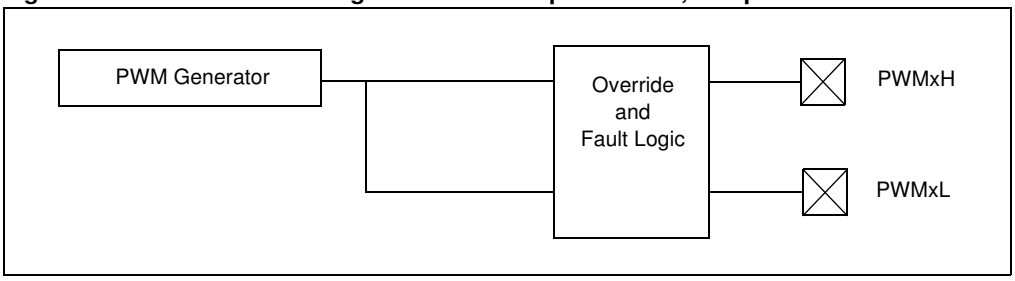


Figure 15-18: PWM Block Diagram for One Output Pin Pair, Independent Mode



15.8 PWM Output Override

The PWM output override bits allow the user to manually drive the PWM I/O pins to specified logic states independent of the duty cycle comparison units. The PWM override bits are useful when controlling various types of electrically commutated motors.

All control bits associated with the PWM output override function are contained in the OVDCON register. The upper half of the OVDCON register contains 8 bits, POVDxx, that determine which PWM I/O pins will be overridden. The lower half of the OVDCON register contains 8 bits, POUTxx, that determine the state of the PWM I/O pin when it is overridden via the POVDxx bit.

The POVD bits are active-low control bits. When the POVD bits are set, the corresponding POUTxx bit will have no effect on the PWM output. When one of the POVD bits is cleared, the output on the corresponding PWM I/O pin will be determined by the state of the POUT bit. When a POUT bit is set, the PWM pin will be driven to its active state. When the POUT bit is cleared, the PWM pin will be driven to its inactive state.

15.8.1 Override Control for Complementary Output Mode

The PWM module will not allow certain overrides when a pair of PWM I/O pins are operating in the Complementary mode. (PMODx = 0) The module will not allow both pins in the output pair to become active simultaneously. The high-side pin in each output pair will always take priority.

Note:	Dead time insertion is still performed when PWM channels are overridden manually.

15.8.2 Override Synchronization

If the OSYNC bit is set (PWMCON2<1>), all output overrides performed via the OVDCON register will be synchronized to the PWM time base. Synchronous output overrides will occur at the following times:

- Edge aligned mode, when PTMR is zero.
- Center aligned modes, when PTMR is zero, or
- When the value of PTMR matches PTPER.

The override synchronization function, when enabled, can be used to avoid unwanted narrow pulses on the PWM output pins.

15.8.3 Output Override Examples

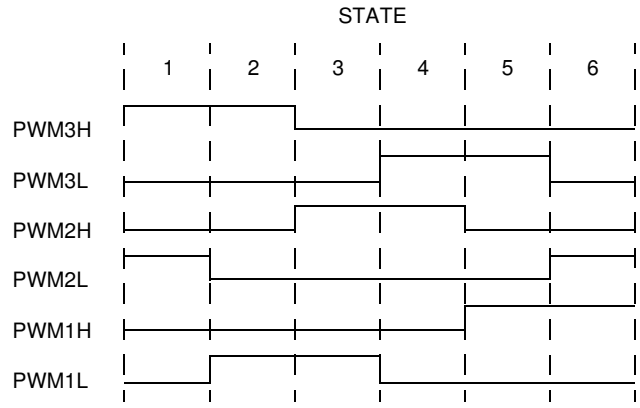
Figure 15-19 shows an example of a waveform that might be generated using the PWM output override feature. The Figure shows a six-step commutation sequence for a BLDC motor. The motor is driven through a 3-phase inverter as shown in Figure 15-13. When the appropriate rotor position is detected, the PWM outputs are switched to the next commutation state in the sequence. In this example, the PWM outputs are driven to specific logic states. The OVDCON register values used to generate the signals in Figure 15-19 are given in Table 15-6.

The PWM duty cycle registers may be used in conjunction with the OVDCON register. The duty cycle registers controls the current delivered to the load and the OVDCON register controls the commutation. Such an example is shown in Figure 15-20. The OVDCON register values used to generate the signals in Figure 15-20 are given in Table 15-7.

Table 15-6: PWM Output Override Example #1

State	OVDCON<15:8>	OVDCON<7:0>
1	00000000b	00100100b
2	00000000b	00100001b
3	00000000b	00001001b
4	00000000b	00011000b
5	00000000b	00010010b
6	00000000b	00000110b

Figure 15-19: PWM Output Override Example #1

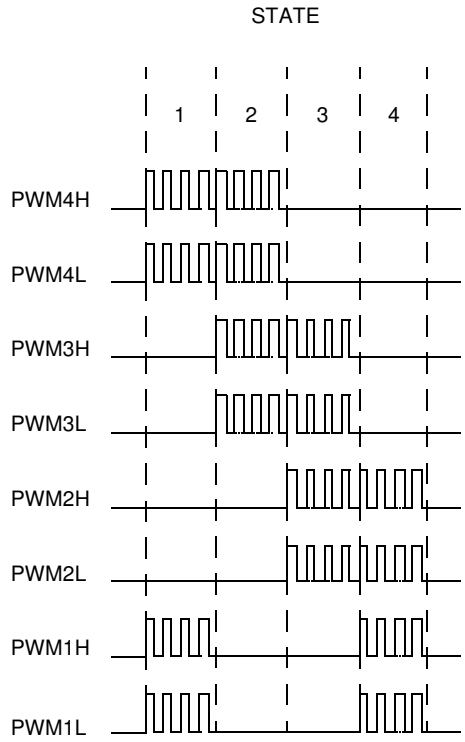


Note: Switching times between states 1-6 are controlled by user software. The state switch is controlled by writing a new value to OVDCON.

Table 15-7: PWM Output Override Example #2

State	OVDCON<15:8>	OVDCON<7:0>
1	11000011b	00000000b
2	11110000b	00000000b
3	00111100b	00000000b
4	00001111b	00000000b

Figure 15-20: PWM Output Override Example #2



Note: Switching times between states 1-4 are controlled by user software. The state switch is controlled by writing a new value to OVDCON. The PWM outputs are operated in the independent mode for this example.

15.9 PWM Output and Polarity Control

The PENxx control bits in PWMCON1 enable each PWM output pin for use by the module. When a pin is enabled for PWM output, the PORT and TRIS registers controlling the pin are disabled.

In addition to the PENxx control bits, there are three device configuration bits in the FBORPOR device configuration register that provide PWM output pin control.

- HPOL configuration bit
- LPOL configuration bit
- PWMPIN configuration bit

These three configuration bits work in conjunction with the PWM enable bits (PENxx) located in PWMCON1. The configuration bits ensure that the PWM pins are in the correct states after a device reset occurs.

15.9.1 Output Polarity Control

The polarity of the PWM I/O pins is set during device programming via the HPOL and LPOL configuration bits in the FBORPOR Device Configuration register. The HPOL configuration bit sets the output polarity for the high-side PWM outputs PWM1H-PWM4H. The LPOL configuration bit sets the output polarity for the low-side PWM outputs PWM1L-PWM 4L.

If the polarity configuration bit is programmed to a '1', the corresponding PWM I/O pins will have active-high output polarity. If the polarity configuration bit is programmed to a '0', then the corresponding PWM pins will have active-low polarity.

15.9.2 PWM Output Pin Reset States

The PWMPIN configuration bit determines the behavior of the PWM output pins on a device reset and can be used to eliminate external pull-up/pull-down resistors connected to the devices controlled by the PWM module.

If the PWMPIN configuration bit is programmed to a '1', the PENxx control bits will be cleared on a device reset. Consequently, all PWM outputs will be tri-stated and controlled by the corresponding PORT and TRIS registers.

If the PWMPIN configuration bit is programmed to a '0', the PENxx control bits will be set on a device reset. All PWM pins will be enabled for PWM output at the device reset and will be at their inactive states as defined by the HPOL and LPOL configuration bits.

15.10 PWM Fault Pins

There are two Fault pins, $\overline{\text{FLTA}}$ and $\overline{\text{FLTB}}$, associated with the PWM module. When asserted, these pins can optionally drive each of the PWM I/O pins to a defined state. This action takes place without software intervention so fault events can be managed quickly.

The Fault pins may have other multiplexed functions depending on the dsPIC device variant. When used as a fault input, each Fault pin is readable via its corresponding PORT register. The FLTA and FLTB pins function as active low inputs so that it is easy to wire-OR many sources to the same input through an external pull-up resistor. When not used with the PWM module, these pins may be used as general purpose I/O or another multiplexed function. Each Fault pin has its own interrupt vector, Interrupt Flag bit, Interrupt Enable bit and Interrupt Priority bits associated with it.

The function of the $\overline{\text{FLTA}}$ pin is controlled by the FLTACON register and the function of the $\overline{\text{FLTB}}$ pin is controlled by the FLTBCON register.

15.10.1 Fault Pin Enable Bits

The FLTACON and FLTBCON registers each have 4 control bits, FxEN1-FxEN4, that determine whether a particular pair of PWM I/O pins is to be controlled by the fault input pin. To enable a specific PWM I/O pin pair for fault overrides, the corresponding bit should be set in the FLTACON or FLTBCON register.

If all enable bits are cleared in the FLTACON or FLTBCON registers, then that fault input pin has no effect on the PWM module and no fault interrupts will be produced.

15.10.2 Fault States

The FLTACON and FLTBCON special function registers each have 8 bits that determine the state of each PWM I/O pin when the fault input pin becomes active. When these bits are cleared, the PWM I/O pin will be driven to the inactive state. If the bit is set, the PWM I/O pin will be driven to the active state. The active and inactive states are referenced to the polarity defined for each PWM I/O pin (set by HPOL and LPOL device configuration bits).

A special case exists when a PWM module I/O pair is in the Complementary mode and both pins are programmed to be active on a fault condition. The high-side pin will always have priority in the Complementary mode so that both I/O pins cannot be driven active simultaneously.

15.10.3 Fault Input Modes

Each of the fault input pins has two modes of operation:

- **Latched Mode:** When the fault pin is driven low, the PWM outputs will go to the states defined in the FLTxCON register. The PWM outputs will remain in this state until the fault pin is driven high AND the corresponding interrupt flag (FLTxIF) has been cleared in software. When both of these actions have occurred, the PWM outputs will return to normal operation at the beginning of the next PWM period or half-period boundary regardless of the Immediate Update Enable bit value (IUE). If the interrupt flag is cleared before the fault condition ends, the PWM module will wait until the fault pin is no longer asserted to restore the outputs.
- **Cycle-by-Cycle Mode:** When the fault input pin is driven low, the PWM outputs will remain in the defined fault states for as long as the fault pin is held low. After the fault pin is driven high, the PWM outputs will return to normal operation at the beginning of the following PWM period (or half-period boundary in center aligned modes) even when immediate updates are enabled.

The operating mode for each fault input pin is selected using the FLTAM and FLTBM control bits (FLTACON<7> and FLTBCON<7>).

15.10.3.1 Entry Into a Fault Condition

When a fault pin is enabled and driven low, the PWM pins are immediately driven to their programmed fault states regardless of the values in the PDCx and OVDCON registers. The fault action has priority over all other PWM control registers.

15.10.3.2 Exit From a Fault Condition

A fault condition must be cleared by the external circuitry driving the fault input pin high and clearing the fault interrupt flag (Latched mode only). After the fault pin condition has been cleared, the PWM module will restore the PWM output signals on the next PWM period or half-period boundary. For edge aligned PWM generation, the PWM outputs will be restored when PTMR = 0. For center aligned PWM generation, the PWM outputs will be restored when PTMR = 0 or PTMR = PTPER, whichever event occurs first.

An exception to these rules will occur when the PWM time base is disabled (PTEN = 0). If the PWM time base is disabled, the PWM module will restore the PWM output signals immediately after the fault condition has been cleared.

15.10.4 Fault Pin Priority

If both fault input pins have been assigned to control a particular pair of PWM pins, the fault states programmed for the FLTA input pin will take priority over the FLTB input pin.

One of two actions will take place when the Fault A condition has been cleared. If the FLTB input is still asserted, the PWM outputs will return to the states programmed in the FLTBCON register on the next period or half-period boundary. If the FLTB input is not asserted, the PWM outputs will return to normal operation on the next period or half-period boundary.

Note:	When the FLTA pin is programmed for Latched mode, the PWM outputs will not return to the Fault B states or normal operation until the Fault A interrupt flag has been cleared and the FLTA pin is de-asserted.

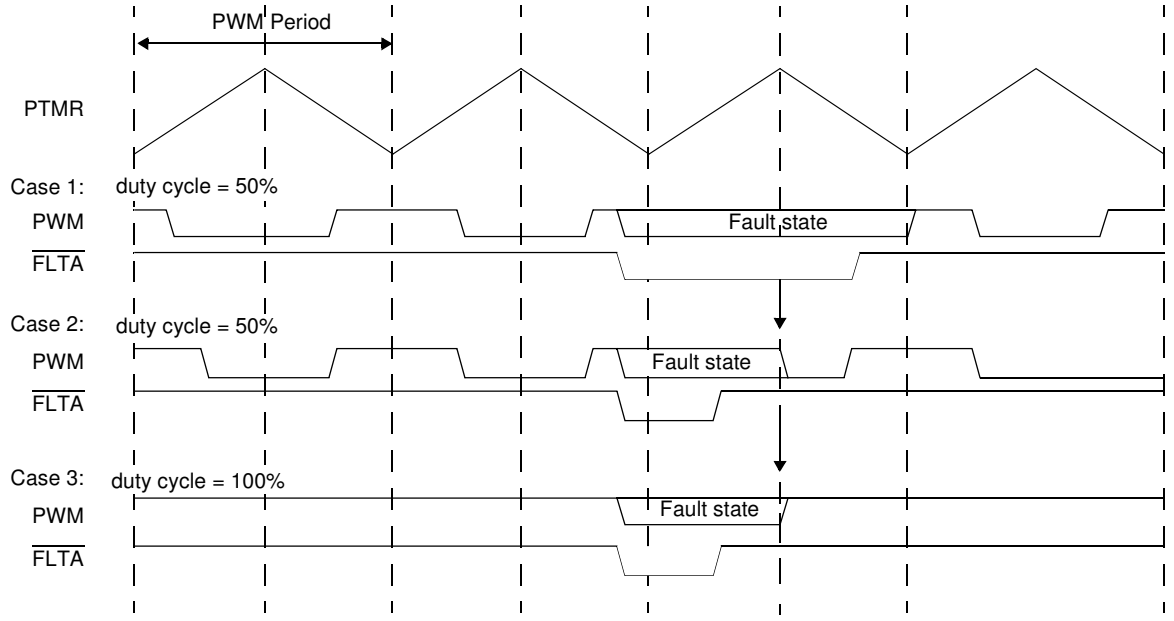
15.10.5 Fault Pin Software Control

Each of the fault pins can be controlled manually in software. Since each fault input is shared with a PORT I/O pin, the PORT pin can be configured as an output by clearing the corresponding TRIS bit. When the PORT bit for the pin is cleared, the fault input will be activated.

Note:	The user should exercise caution when controlling the fault inputs in software. If the TRIS bit for the fault pin is cleared, then the fault input cannot be driven externally.

15.10.6 Fault Timing Examples

Figure 15-21: Example Fault Timing, Cycle-by-Cycle Mode



Note: Arrows indicate the time when normal PWM operation is restored.

Figure 15-22: Example Fault Timing, Latched Mode

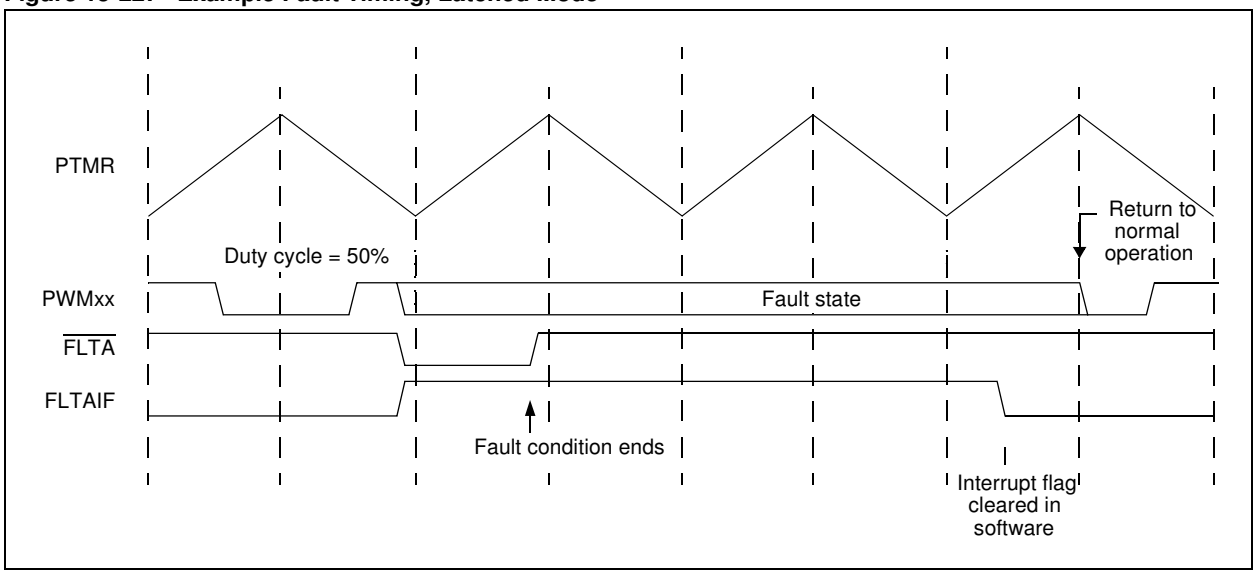
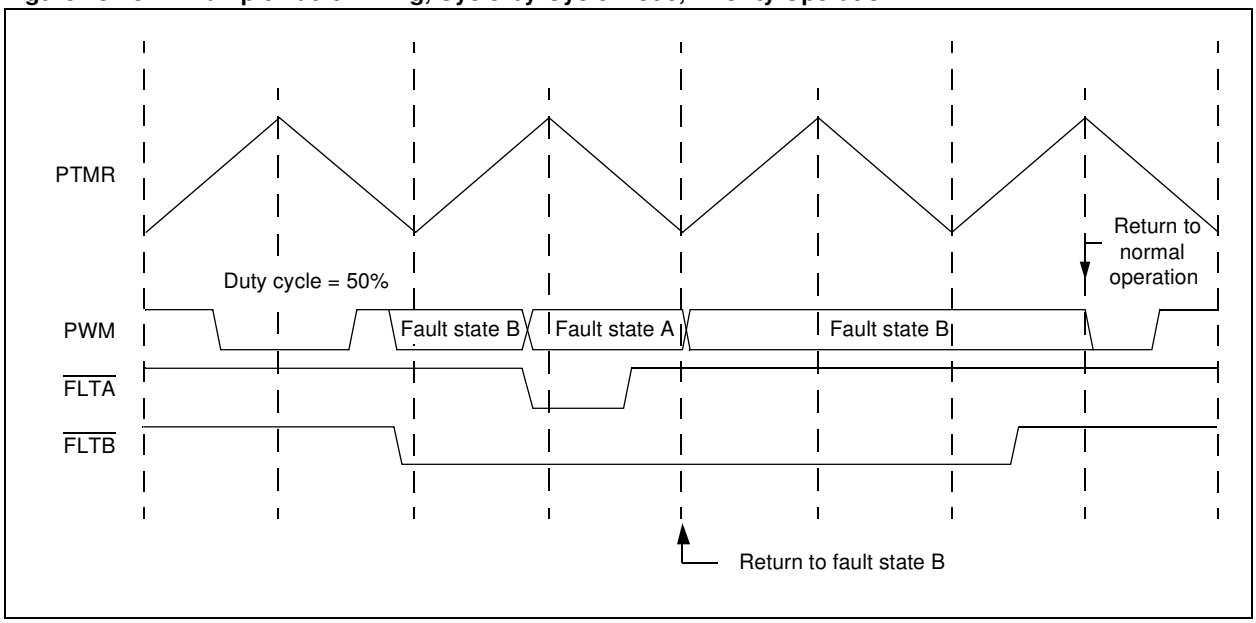


Figure 15-23: Example Fault Timing, Cycle-by-Cycle Mode, Priority Operation



15.11 PWM Update Lockout

In some applications, it is important that all duty cycle and period registers be written before the new values take effect. The update disable feature allows the user to specify when new duty cycle and period values can be used by the module. The PWM update lockout feature is enabled by setting the UDIS control bit (PWMCON2<0>).

The UDIS bit affects all duty cycle registers, PDC1-PDC4, and the PWM time base period buffer, PTPER. To perform an update lockout, the user should perform the following steps:

- Set the UDIS bit.
- Write all duty cycle registers and PTPER, if applicable.
- Clear the UDIS bit to re-enable updates.

Note:	Immediate updates must be disabled (IUE = 0) in order to use the PWM update lockout feature.

15.12 PWM Special Event Trigger

The PWM module has a special event trigger that allows A/D conversions to be synchronized to the PWM time base. The A/D sampling and conversion time may be programmed to occur at any point within the PWM period. The special event trigger allows the user to minimize the delay between the time when A/D conversion results are acquired and the time when the duty cycle value is updated.

The PWM special event trigger has one SFR, SEVTCMP, and four postscaler control bits (SEVOPS<3:0>) to control its operation. The PTMR value for which a special event trigger should occur is loaded into the SEVTCMP register.

When the PWM time base is in an Up/Down Counting mode, an additional control bit is required to specify the counting phase for the special event trigger. The count phase is selected using the SEVTDIR control bit in the MSb of SEVTCMP. If the SEVTDIR bit is cleared, the special event trigger will occur on the upward counting cycle of the PWM time base. If the SEVTDIR bit is set, the special event trigger will occur on the downward count cycle of the PWM time base. The SEVTDIR control bit has no effect unless the PWM time base is configured for an Up/Down Counting mode.

15.12.1 Special Event Trigger Enable

The PWM module will always produce the special event trigger signal. This signal may optionally be used by the A/D module. Refer to **Section Section 17. "10-bit A/D Converter"** for more information on using the special event trigger.

15.12.2 Special Event Trigger Postscaler

The PWM special event trigger has a postscaler that allows a 1:1 to 1:16 postcale ratio. The postscaler is useful when synchronized A/D conversions do not need to be performed during every PWM cycle. The postscaler is configured by writing the SEVOPS<3:0> control bits in the PWMCON2 SFR.

The special event output postscaler is cleared on the following events:

- Any write to the SEVTCMP register.
- Any device reset.

15.13 Operation in Device Power Saving Modes

15.13.1 PWM Operation in Sleep mode

When the device enters Sleep mode, the system clock is disabled. Since the clock for the PWM time base is derived from the system clock source (TCY), it will also be disabled. All enabled PWM output pins will be frozen in the output states that were in effect prior to entering Sleep.

If the PWM module is used to control a load in a power application, it is the user's responsibility to put the PWM module outputs into a 'safe' state prior to executing the `PWRSAV` instruction. Depending on the application, the load may begin to consume excessive current when the PWM outputs are frozen in a particular output state. For example, the OVDCON register can be used to manually turn off the PWM output pins as shown in the code example below.

```
; This code example drives all PWM pins to the inactive state
; before executing the PWRSAV instruction.

   CLR      OVDCON       ; Force all PWM outputs inactive
   PWRSAV   #0           ; Put the device in SLEEP mode
   SETM.B   OVDCONH      ; Set POVD bits when device wakes.
```

The Fault A and Fault B input pins, if enabled to control the PWM pins via the FLTxCON registers, will continue to function normally when the device is in Sleep mode. If one of the fault pins is driven low while the device is in Sleep, the PWM outputs will be driven to the programmed fault states in the FLTxCON register.

The fault input pins also have the ability to wake the CPU from Sleep mode. If the fault interrupt enable bit is set (FLTxIE = 1), then the device will wake from Sleep when the fault pin is driven low. If the fault pin interrupt priority is greater than the current CPU priority, then program execution will start at the fault pin interrupt vector location upon wake-up. Otherwise, execution will continue from the next instruction following the PWRSAV instruction.

15.13.2 PWM Operation in Idle Mode

When the device enters Idle mode, the system clock sources remain functional and the CPU stops executing code. The PWM module can optionally continue to operate in Idle mode.The PTSIDL bit (PTCON<13>) selects if the PWM module will stop in Idle mode or continue to operate normally.

If PTSIDL = 0, the module will operate normally when the device enters Idle mode. The PWM time base interrupt, if enabled, can be used to wake the device from Idle. If the PWM time base interrupt enable bit is set (PTIE = 1), then the device will wake from Idle when the PWM time base interrupt is generated. If the PWM time base interrupt priority is greater than the current CPU priority, then program execution will start at the PWM interrupt vector location upon wake-up. Otherwise, execution will continue from the next instruction following the PWRSAV instruction.

If PTSIDL = 1, the module will stop in Idle mode. If the PWM module is programmed to stop in Idle mode, the operation of the PWM outputs and fault input pins will be the same as the operation in Sleep mode. (See discussion in **Section 15.13.1 "PWM Operation in Sleep mode"**.)

15.14 Special Features for Device Emulation

The PWM module has a special feature to support the debugging environment. All enabled PWM pins can be optionally tri-stated when the hardware emulator or debugger device is halted to examine memory contents. The user should install pull-up or pull-down resistors to ensure the PWM outputs are driven to the correct state when device execution is halted.

The function of the PWM output pins at a device Reset and the output pin polarity is determined by three device configuration bits (see **Section 15.9 "PWM Output and Polarity Control"**). The hardware debugger or emulation tool provides a method to change the values of these configuration bits. Please refer to the tool's user's manual for more information.

Table 15-8: Registers Associated with the 8-Output PWM Module

Name	ADR	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Reset
INTCON1	0080	NSTDIS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000 0000 0000 0000
INTCON2	0082	ALTIVT	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000 0000 0000 0000
IFS2	0088	—	—	—	FLTBIF	FLTAIF	—	—	—	PWMIF	—	—	—	—	—	—	—	0000 0000 0000 0000
IEC2	0090	—	—	—	FLTBIE	FLTAIE	—	—	—	PWMIE	—	—	—	—	—	—	—	0000 0000 0000 0000
IPC9	00A6	—	PWMIP<2:0>			—	—	—	—	—	—	—	—	—	—	—	—	0100 0100 0100 0100
IPC10	00A8	—	FLTAIP<2:0>			—	—	—	—	—	—	—	—	—	—	—	—	0100 0100 0100 0100
IPC11	00AA	—	—	—	—	—	—	—	—	—	—	—	—	—	FLTBIP<2:>			0000 0000 0000 0000
PTCON	01C0	PTEN	—	PTSIDL	—	—	—	—	—	PTOPS<3:0>				PTCKPS<1:0>		PTMOD<1:0>		0000 0000 0000 0000
PTMR	01C2	PTDIR	PWM Time Base register															0000 0000 0000 0000
PTPER	01C4	—	PWM Time Base Period register															0111 1111 1111 1111
SEVTCMP	01C6	SEVTDIR	PWM Special Event Compare register															0000 0000 0000 0000
PWMCON1	01C8	—	—	—	—	PMOD4	PMOD3	PMOD2	PMOD1	PEN4H	PEN3H	PEN2H	PEN1H	PEN4L	PEN3L	PEN2L	PEN1L	0000 0000 0000 0000
PWMCON2	01CA	—	—	—	—	SEVOPS<3:0>				—	—	—	—	—	IUE	OSYNC	UDIS	0000 0000 0000 0000
DTCON1	01CC	DTBPS<1:0>		Dead Time B Value register						DTAPS<1:0>		Dead Time A Value register						0000 0000 0000 0000
DTCON2	01CE	—	—	—	—	—	—	—	—	DTS4A	DTS4I	DTS3A	DTS3I	DTS2A	DTS2I	DTS1A	DTS1I	0000 0000 0000 0000
FLTACON	01D0	FAOV4H	FAOV4L	FAOV3H	FAOV3L	FAOV2H	FAOV2L	FAOV1H	FAOV1L	FLTAM	—	—	—	FAEN4	FAEN3	FAEN2	FAEN1	0000 00-0 0000 0000
FLTBCON	01D2	FBOV4H	FBOV4L	FBOV3H	FBOV3L	FBOV2H	FBOV2L	FBOV1H	FBOV1L	FLTBM	—	—	—	FBEN4	FBEN3	FBEN2	FBEN1	0000 0000 0000 0000
OVDCON	01D4	POVD4H	POVD4L	POVD3H	POVD3L	POVD2H	POVD2L	POVD1H	POVD1L	POUT4H	POUT4L	POUT3H	POUT3L	POUT2H	POUT2L	POUT1H	POUT1L	1111 1111 00-0 0000
PDC1	01D6	PWM Duty Cycle #1 register																0000 0000 0000 0000
PDC2	01D8	PWM Duty Cycle #2 register																0000 0000 0000 0000
PDC3	01DA	PWM Duty Cycle #3 register																0000 0000 0000 0000
PDC4	01DC	PWM Duty Cycle #4 register																0000 0000 0000 0000

Note 1: Reset state of PENxx control bits depends on the state of the PWMPIN device configuration bit.

2: Shaded register and bit locations not implemented for the 6-output MCPWM module.

3: The IUE bit is not implemented on the dsPIC30F6010 device.

Table 15-9: Registers Associated with the 6-Output PWM Module

Name	ADR	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Reset
INTCON1	0080	NSTDIS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000 0000 0000 0000
INTCON2	0082	ALTIVT	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000 0000 0000 0000
IFS2	0088	—	—	—	—	FLATIF	—	—	—	PWMIF	—	—	—	—	—	—	—	0000 0000 0000 0000
IEC2	0090	—	—	—	—	FLTAIE	—	—	—	PWMIE	—	—	—	—	—	—	—	0000 0000 0000 0000
IPC9	00A6	—	PWMIP<2:0>			—	—	—	—	—	—	—	—	—	—	—	—	0100 0100 0100 0100
IPC10	00A8	—	FLTAIP<2:0>			—	—	—	—	—	—	—	—	—	—	—	—	0100 0100 0100 0100
PTCON	01C0	PTEN	—	PTSIDL	—	—	—	—	—	PTOPS<3:0>				PTCKPS<1:0>		PTMOD<1:0>		0000 0000 0000 0000
PTMR	01C2	PTDIR	PWM Time Base register															0000 0000 0000 0000
PTPER	01C4	—	PWM Time Base Period register															0111 1111 1111 1111
SEVTCMP	01C6	SEVTDIR	PWM Special Event Compare register															0000 0000 0000 0000
PWMCON1	01C8	—	—	—	—	—	PMOD3	PMOD2	PMOD1	—	PEN3H	PEN2H	PEN1H	—	PEN3L	PEN2L	PEN1L	0000 0000 0000 0000
PWMCON2	01CA	—	—	—	—	—				—	—	—	—	—	IUE	OSYNC	UDIS	0000 0000 0000 0000
DTCON1	01CC	—	—	—	—	—	—	—	—	DTAPS<1:0>		Dead Time A Value register						0000 0000 0000 0000
Reserved	01CE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
FLTACON	01D0	—	—	FAOV3H	FAOV3L	FAOV2H	FAOV2L	FAOV1H	FAOV1L	FLTAM	—	—	—	FAEN4	FAEN3	FAEN2	FAEN1	0000 00-0 0000 0000
Reserved	01D2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
OVDCON	01D4	—	—	POVD3H	POVD3L	POVD2H	POVD2L	POVD1H	POVD1L	—	—	POUT3H	POUT3L	POUT2H	POUT2L	POUT1H	POUT1L	1111 1111 00-0 0000
PDC1	01D6	PWM Duty Cycle #1 register																0000 0000 0000 0000
PDC2	01D8	PWM Duty Cycle #2 register																0000 0000 0000 0000
PDC3	01DA	PWM Duty Cycle #3 register																0000 0000 0000 0000

Note 1: Reset state of PENxx control bits depends on the state of the PWMPIN device configuration bit.

2: Shaded register and bit locations not implemented for the 6-output MCPWM module.

3: The IUE bit is not implemented on the dsPIC30F6010 device.

15.15 Related Application Notes

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC30F Product Family, but the concepts are pertinent, and could be used with modification and possible limitations. The current application notes related to the MCPWM module are:

Title	Application Note #
PIC18CXXX/PIC16CXXX Servomotor	AN696
Using the dsPIC30F for Sensorless BLDC Control	AN901
Using the dsPIC30F for Vector Control of an ACIM	AN908
Sensored BLDC Motor Control Using dsPIC30F2010	AN957
An Introduction to AC Induction Motor Control Using the dsPIC30F MCU	AN984

Note: Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC30F Family of devices.